

# Micro-Electro-Mechanical Systems (MEMS) Technology

by



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# Summary

- The Sandia Ultra-planar, Multi-level MEMS Technology (*SUMMiT*)
- SUMMiT V Fabrication Process
- Integrated MEMS Systems IMEMS



# The Sandia Ultra-planar, Multi-level MEMS Technology (*SUMMiT*)

- The SUMMiT fabrication process is a four-level polycrystalline silicon surface micromachining process (one ground plane/electrical interconnect and three mechanical layers).
- Polycrystalline silicon (often termed polysilicon, or poly) is an ideal material from which to make microscopic electro-mechanical systems
- Its mechanical properties are excellent: it is stronger than steel, polysilicon has a strength of 2-3 GPa, depending on surface flaws; while steel has a strength of 200MPa - 1GPa



# The Sandia Ultra-planar, Multi-level MEMS Technology (*SUMMiT*)

- It is extremely flexible (the maximum strain before fracture is  $\sim 0.5\%$ ), and does not readily fatigue.
- Most importantly, polysilicon is directly compatible with modern IC fabrication processes. In fact, polysilicon is currently used in virtually all IC fabs as the primary material comprising the gate electrode of transistors.
- Batch fabrication in IC foundries makes it possible to produce MEMS in large volumes at extremely low cost. Because of these advantages, polysilicon surface micromachining is being aggressively pursued and applied by many in the MEMS community.

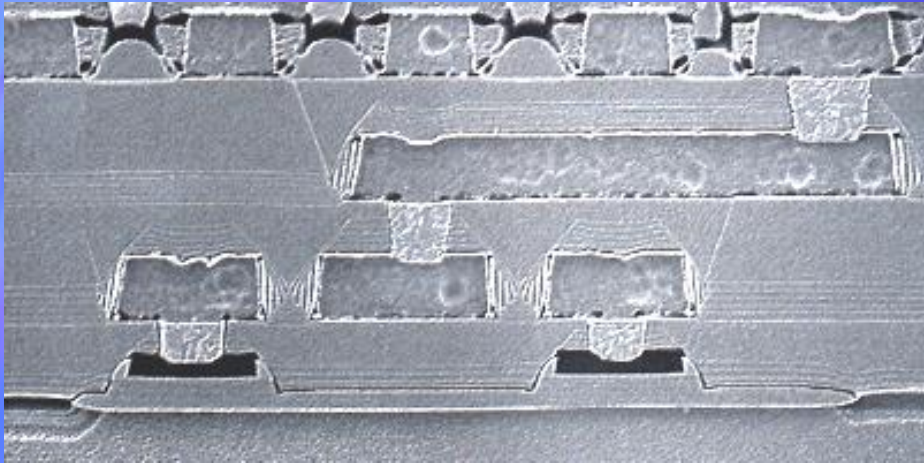


Figure 1. Polysilicon, comprising the gate electrode of the transistor shown in this SEM, is a material in common use in IC fabs across the world. Its deposition and etch properties are very well known.

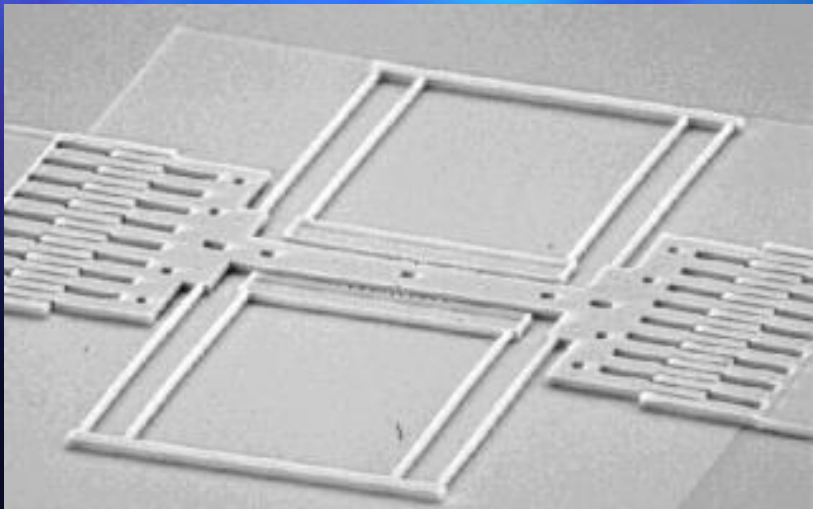
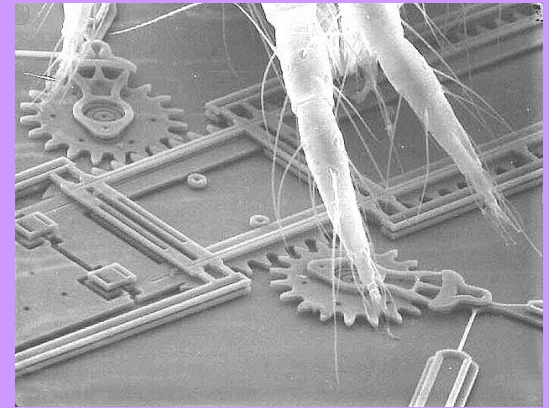
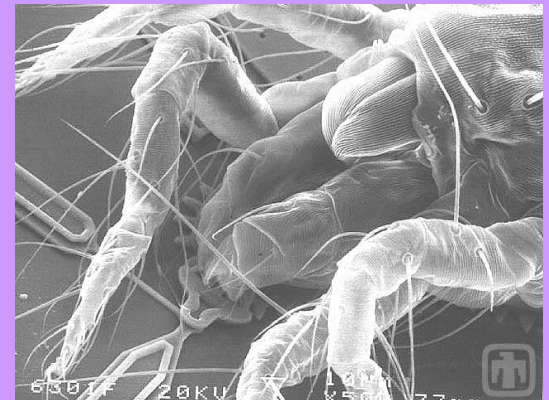


Figure 2. A comb drive actuator is fabricated using a ground plane and a single mechanical layer.



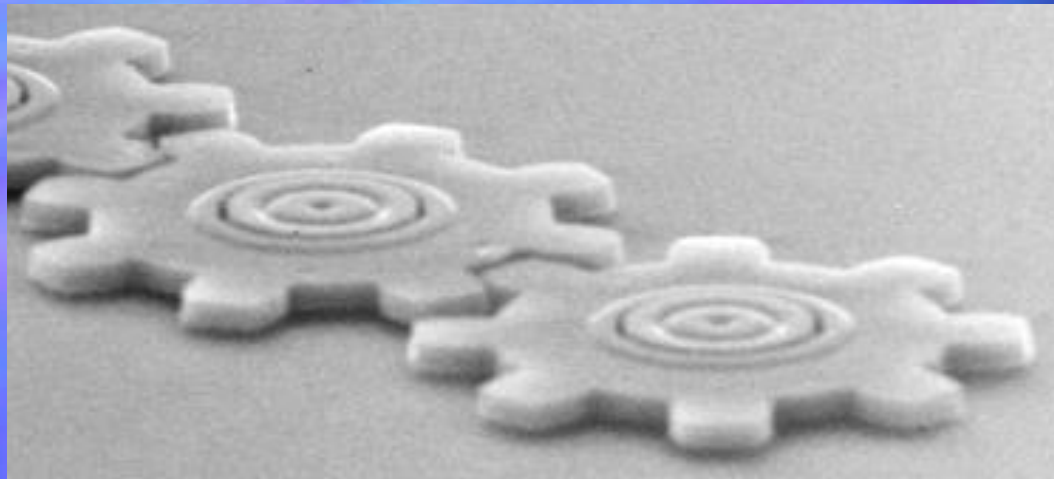
Spider Mite shows scale





# MEMS

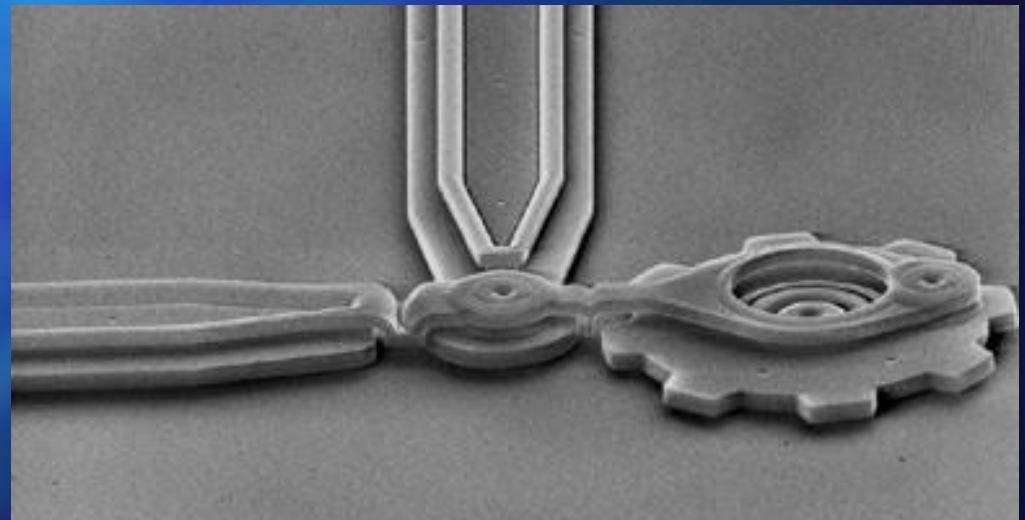
- The complexity of devices that may be created using polysilicon surface micromachining is governed by the number of mechanical layers available in the given fabrication process.
- For example, with a ground plane and one mechanical level (a so-called two-level process), an actuating comb drive may be created.
- With two mechanical levels, one can create mechanisms such as a gear constrained to rotate on a hub, and various types of mirror.
- By adding a third mechanical level, this not only enables the creation of linkages to connect actuators to mechanisms, but opens up an entirely new range of design possibilities that is staggering in scope.



**Figure 3. Two mechanical layers enable the creation of a gear free to rotate on a hub.**



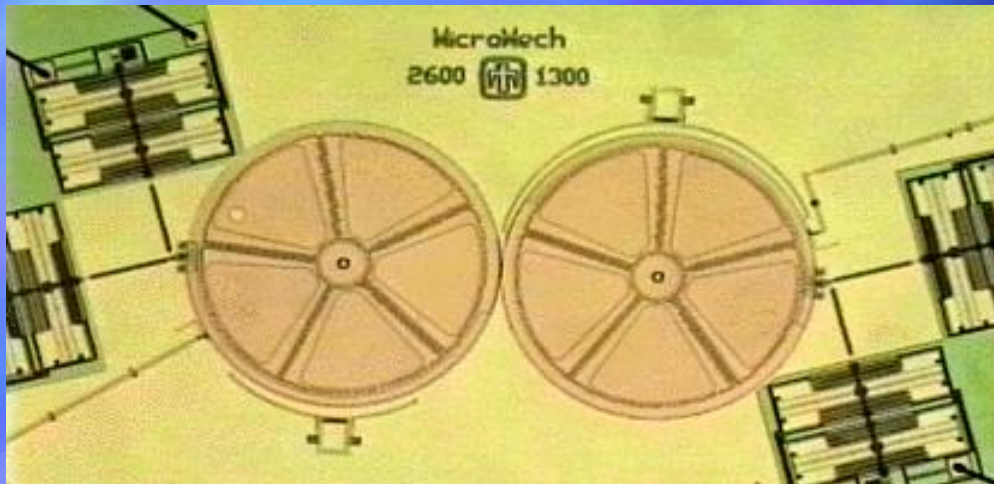
**Figure 4. A third mechanical layer enables an actuator to be linked to a tool, as illustrated by Sandia's microengine.**



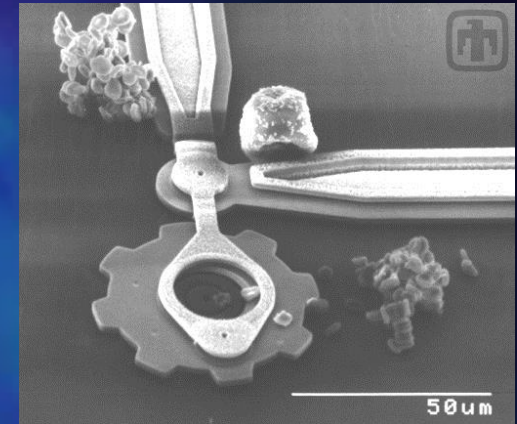
# Residual Stress

- Residual stress can result in the mechanical layers being bowed out of plane.
- Resulting in difficult-to-calibrate devices, non-reproducible devices, or worse yet, non-functioning devices.
- MEMS foundries, even those dealing with only one or two mechanical layers, often find it a challenge to reproducibly reduce polysilicon stress to an acceptable level.
- Sandia has developed a proprietary process by which it maintains stress levels to typically less than 5MPa.
- Meshing gears, each 2000 microns in diameter, have been successfully fabricated and operated.

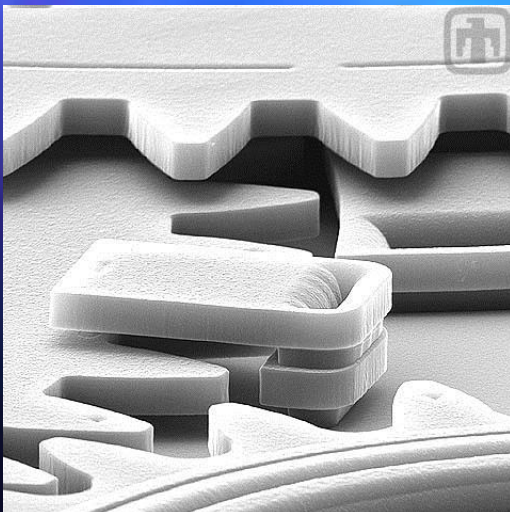




**Figure 5. Flat 2000 micron diameter gears resulting from Sandia's 4-level, low stress, SUMMIT fabrication process.**

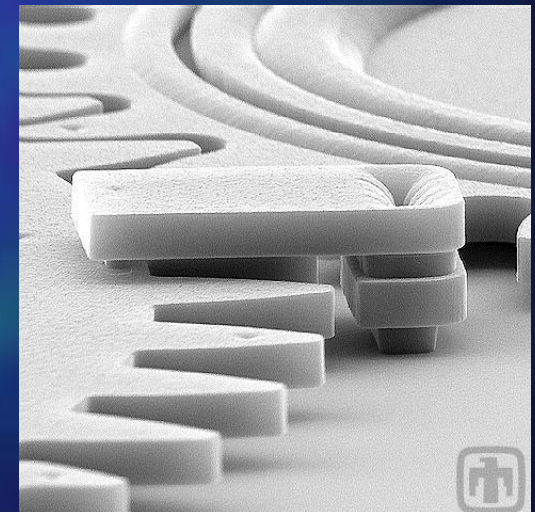


**Grain of pollen and red blood cells**



#### Alignment Clip

**Meshing MEMS gears is a lot like meshing two sheets of paper; they are very thin. Alignment clips are used to help ensure these co-planar gears stay properly meshed.**



# Device Topography

- Device topography can make it difficult to pattern and etch subsequent layers of polysilicon.
- In addition, topography can result in structural artefacts that severely constrain the range of designs that can be successfully implemented.
- To mitigate the problems caused by topography, Sandia has implemented a proprietary planarization method based on Chemical-Mechanical Polishing (CMP).
- This planarization method results in the top layer of poly being planar, enabling far greater design flexibility than in a non-planar process.
- The advanced, planarized, SUMMiT fabrication process allows batch fabrication using only conventional IC processing tools.



# Fabrication Process

- Devices are created using the SUMMiT fabrication process by alternately depositing a film, photolithographically patterning the film, and then performing chemical etching.
- By repeating this process with layers of silicon dioxide and polycrystalline silicon, complex three dimensional shapes can be formed.
- The shapes themselves result from the fabrication process in conjunction with a series of two-dimensional "masks" that define the patterns to be etched.
- The SUMMiT process uses 11 individual masks in the process, about the same number as a relatively simple CMOS IC process.

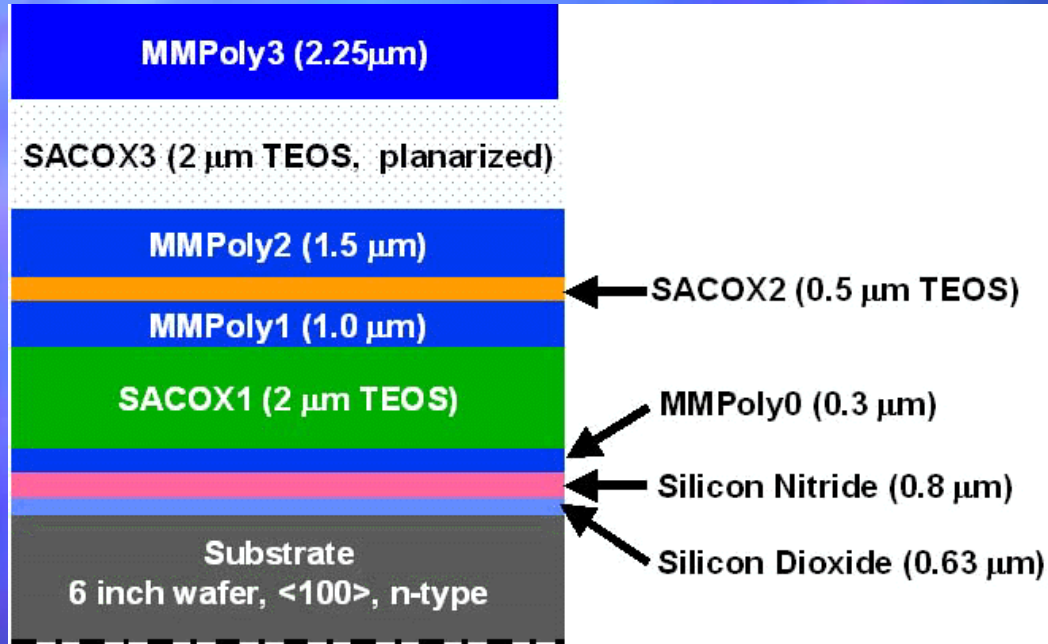


# Fabrication Process

- At the end of the fabrication process, the silicon dioxide is chemically removed
- leaving behind the mechanical structures comprised of polycrystalline silicon.
- Figure 6 shows a cross section schematic of the layers associated with the technology, with no patterning.
- Figure 7 shows the cross section of an actual gear on a hub, along with a pin joint contained in the gear.



Figure 6. Schematic of layers in the SUMMIT process



## Sub-Atmospheric Chemical Vapor Deposition (SACVD)

Using TEOS (tetraethylorthosilicate) and Ozone ( $O_3$ ) chemistry at near-atmospheric pressure, SACVD quickly proved its ability to achieve excellent step coverage, void-free gap-filling and superior planarization characteristics in high aspect ratio structures down to 0.25 micron with high throughput and reliable operation.

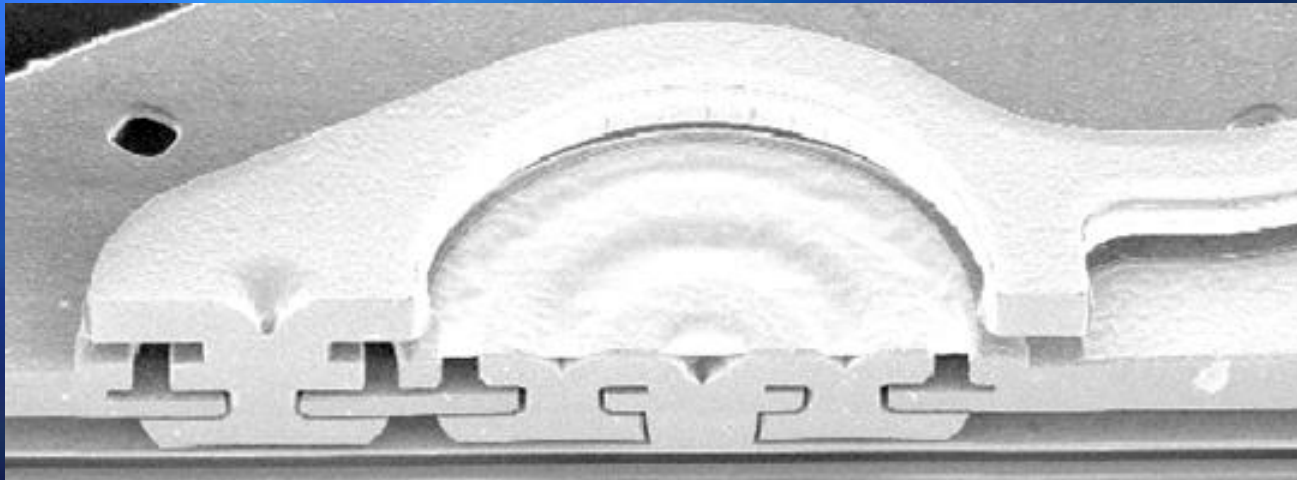
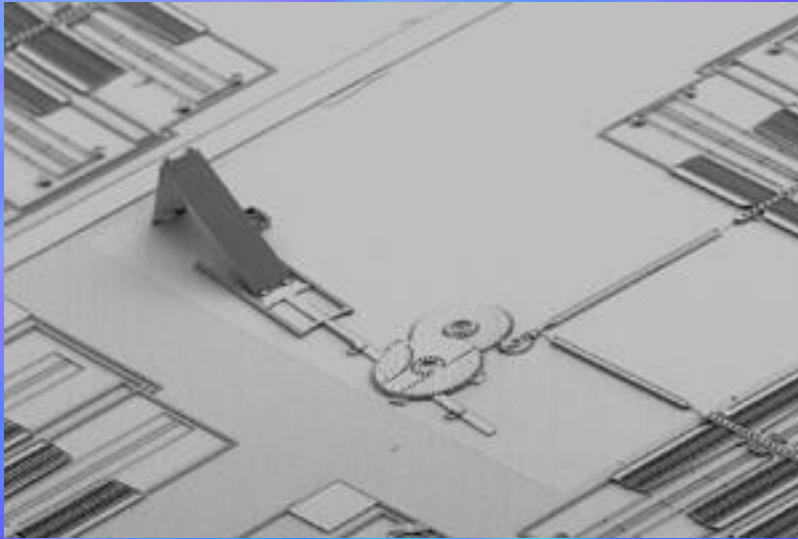


Figure 7. Cross-section of MEMS gear

# MEMS Systems

- Examples of systems created using the SUMMiT fabrication process include a hinged positionable mirror actuated through a transmission by an electrostatic engine (Figure 8)
- An optical shutter whose positioning is enabled by the successful operation of a mechanical lock (Figure 9).
- Many other devices that have already been fabricated using this technology are shown in the following slides.
- These systems are batch fabricated with no piece part assembly required, and are electrostatically actuated only using the on-chip micro-engine
- No external manual probing is required.

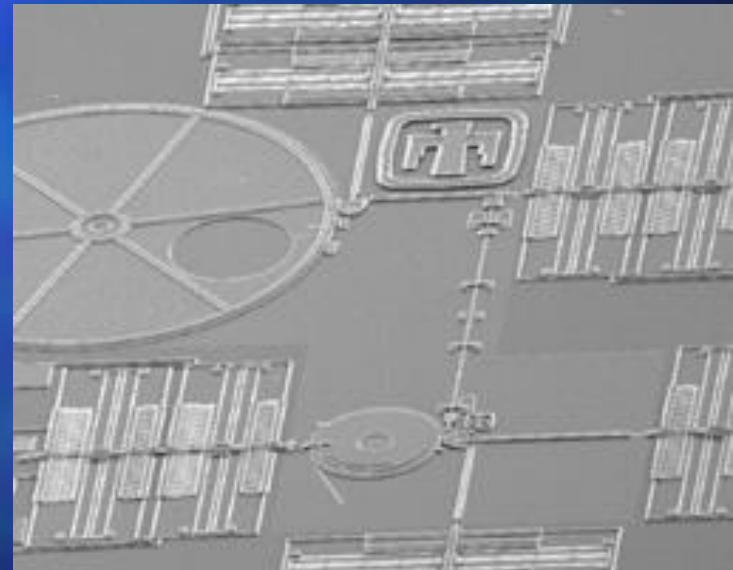


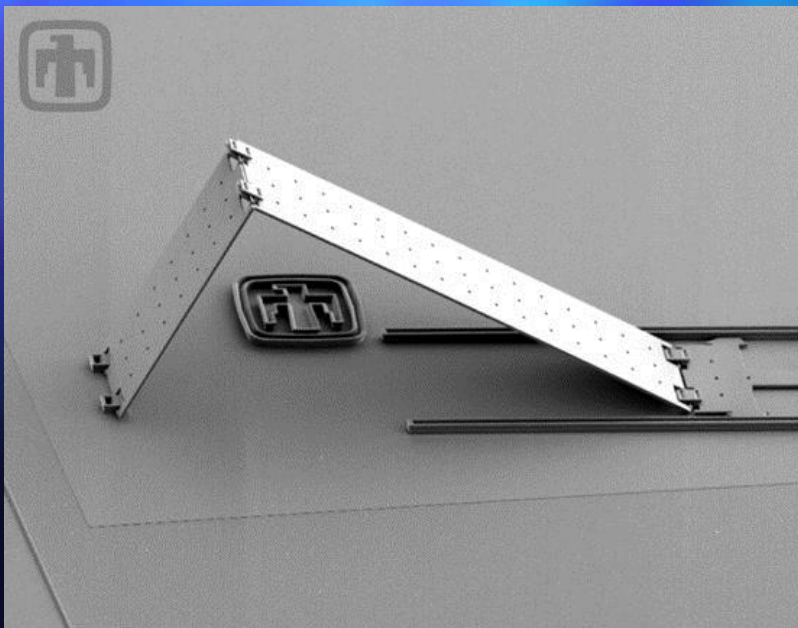
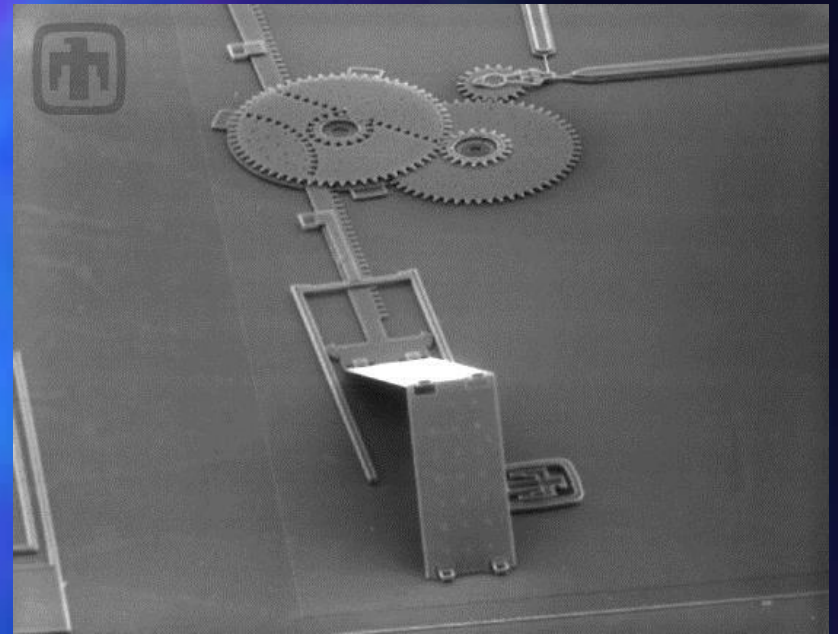
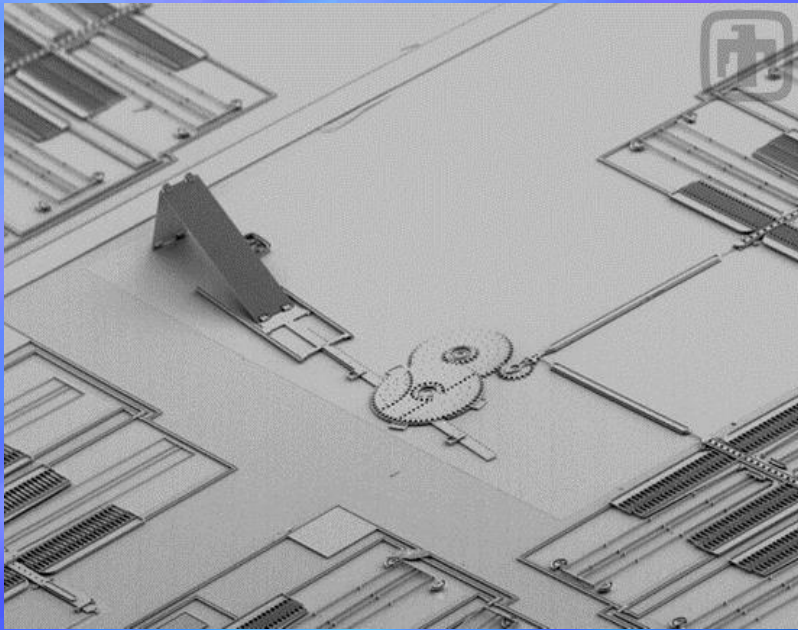


**Figure 8. The torque delivered by the microengine is amplified by the transmission. This in turn pushes a linear rack that positions a hinged mirror.**



**Figure 9. The motion of the optical shutter is constrained by a pin that is removed only by complete rotation of the mechanical lock. The lock is comprised of a pin that is navigated through the maze. Upon the entry of the correct 4-bit code (an anti-reverse ratchet prevents repeated attempts), the hook pulls out the pin constraining the operation of the shutter.**





**Figure 10 Erection of Micro-mirrors  
Different Views**



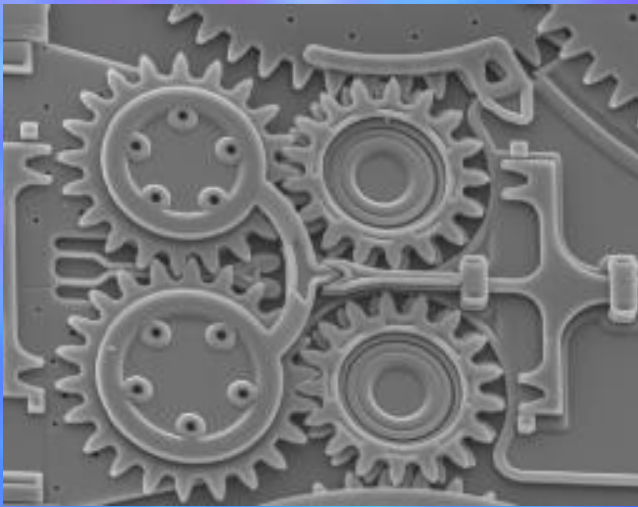
# SUMMiT V Fabrication Process

- The Sandia Ultra-planar, Multi-level MEMS Technology for Five levels (*SUMMiT V*) fabrication process
- This is a five-level polycrystalline silicon surface micromachining process, one ground plane/electrical interconnect and four mechanical layers).
- With SUMMiT V, more advanced systems can be created on moveable platforms (Figure 11).

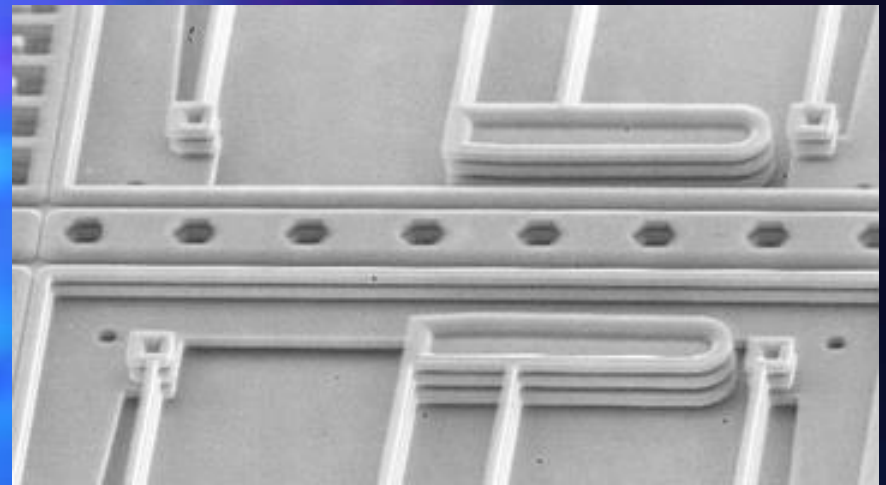


# SUMMiT V Fabrication Process

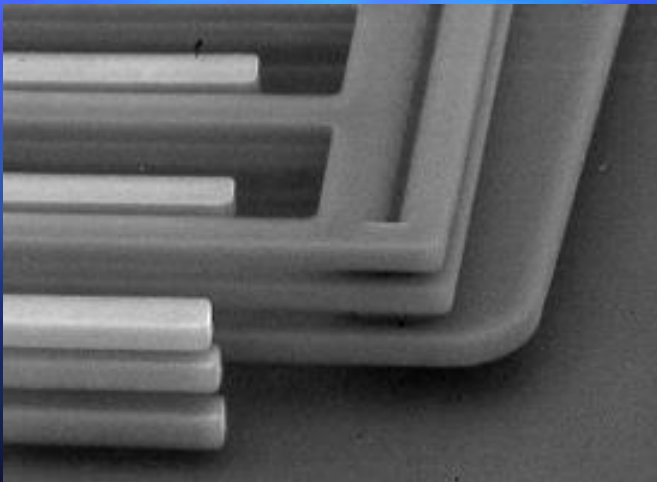
- Much taller devices can be made (up to 12 microns high), enabling greater stiffness and mechanical robustness (Figure 12).
- The additional height can also be used to achieve much greater forces from actuators (Figure 13).
- The design flexibility for a five-level technology is truly enormous, enabling devices for applications that have not yet even been imagined.



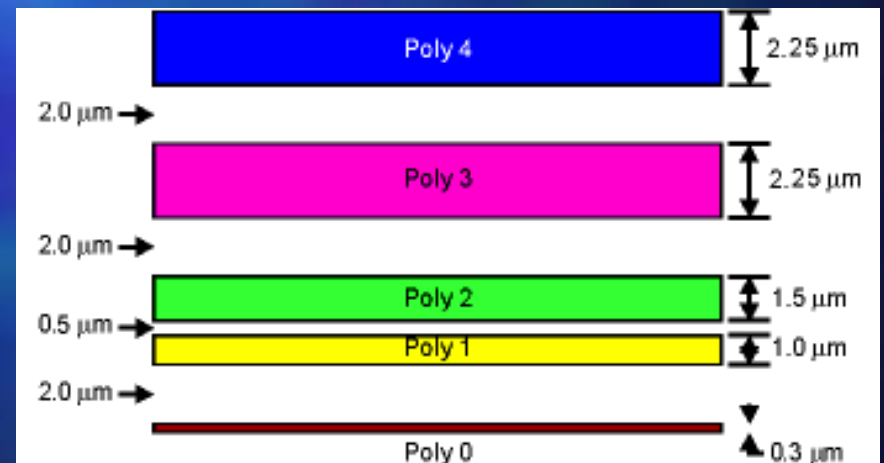
**Figure 11. Meshing gears on a moveable platform.**



**Figure 12. Laminated support springs containing only three mechanical layers result in more than 2 orders of magnitude greater out-of-plane stiffness compared to a single mechanical layer.**



**Figure 13. A laminated comb actuator results in nearly five times the electrostatic force of a single level actuator.**



**Figure 14**

# SUMMiT V Fabrication Process

- Devices are created using the SUMMiT V fabrication process by alternately depositing a film,
- photolithographically patterning the film, and then performing chemical etching.
- By repeating this process with layers of silicon dioxide and polycrystalline silicon, extremely complex, interlocking three-dimensional shapes can be formed.
- The shapes themselves result from the fabrication process in conjunction with a series of two-dimensional "masks" that define the patterns to be etched.



# SUMMiT V Fabrication Process

- The SUMMiT V process uses 14 individual masks in the process, about the same number as many CMOS IC processes.
- At the end of the fabrication process, the silicon dioxide is chemically removed, leaving behind the mechanical structures comprised of polycrystalline silicon.
- Figure 14 shows a cross section schematic of the layers associated with the technology, with no patterning.



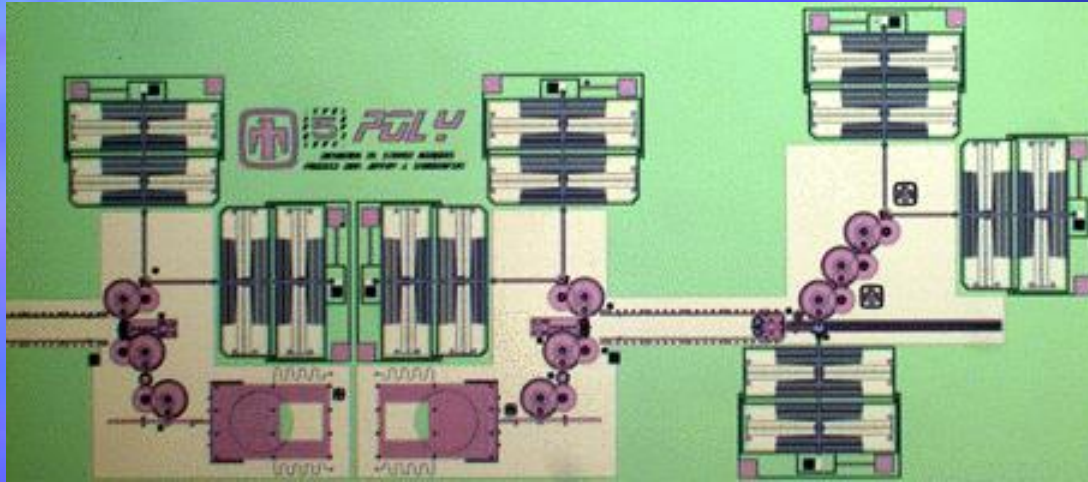


Figure 15. Photograph of microscopic locking device

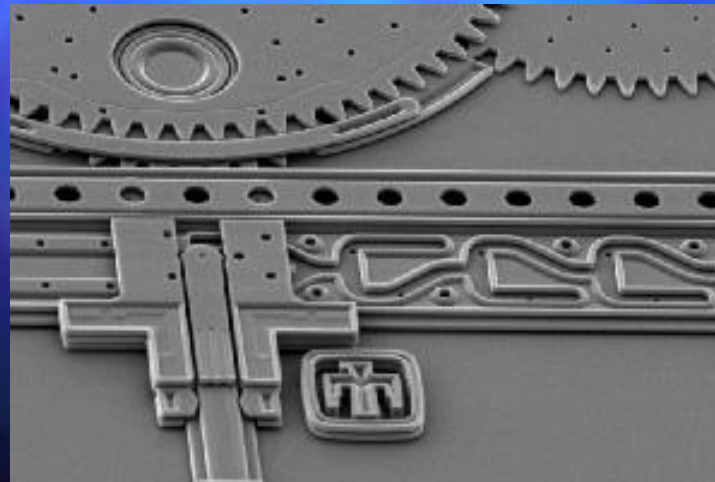
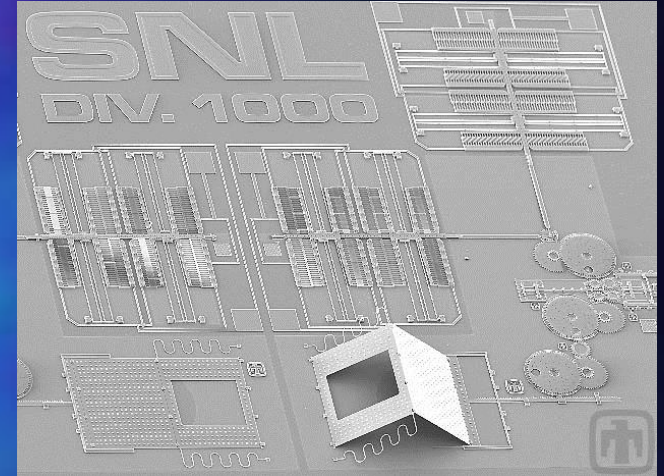


Figure 16. Pin-in-maze

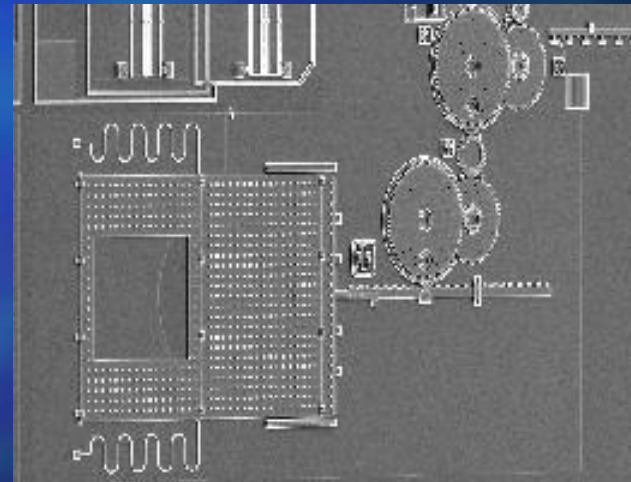


Figure 17. One of the mirrors used for directing laser light

# Proof of Concept MEMS Device

- Using this technology Sandia built an extremely intricate, second-generation microscopic locking device, pictured in Figure 15.
- This is a proof-of-concept safety device that operates through a complex sequence of events that result in unlocking the system.
- The unlocking sequence consists of first entering a 24-bit code to properly guide a pin through a maze, shown in Figure 16.
- If the wrong sequence is entered, an anti-reverse mechanism will cause the system to be safely locked up forever.



# Proof of Concept MEMS Device

- Once the maze has been successfully traversed, two interlocking gears are coupled (see Figure 11 above) which in turn power a gear train that positions two mirrors.
- The mirrors pass an optical signal to electrical circuitry (Figure 17) that then activates the system.
- This entire sequence of events can occur very quickly. The device is a prototype that demonstrates the benefits of using MEMS for safety applications



# Integrated MEMS Systems

## IMEMS

- Integrated MicroElectroMechanical Systems (IMEMS) is a fabrication process that enables both CMOS circuitry and MEMS to be created on the same chip.
- The creation of microsystems (e.g., that sense, think, act, or communicate) often requires electronic circuitry coupled with mechanical elements.
- The monolithic integration of electronic circuitry on the same chip as electro-mechanical devices has many advantages over approaches that involve complex multi-chip packaging schemes.

# Integrated MEMS Systems IMEMS

- Batch fabrication of "systems on a chip" enables very low cost production.
- By reducing the number of components in the system, significantly improved system reliability may be achieved.
- For example, reducing the chip count, eliminating the bond wires connecting electrical to mechanical circuits, and reducing the complexity of the packaging/assembly process all benefit reliability.
- Finally, monolithic integration enables overall system performance, particularly for micro-sensing systems, to be increased by many orders of magnitude by reducing electrical interconnect parasitics, such as capacitance.



# Integration Process Technology

- monolithic integrated CMOS/MEMS technology have motivated numerous fabrication approaches to be pursued by MEMS researchers.
- One approach is to first fabricate the CMOS circuitry, then follow with MEMS processing.
- Unfortunately, the aluminium CMOS interconnects do not withstand the high temperature anneals required to stress-relieve the mechanical polysilicon.

# Integration Process Technology

- The use of tungsten as the interconnect enables higher temperature anneals to be performed, but the anneals then degrade the CMOS performance by altering junction doping profiles.
- Fabrication of the MEMS structures on the surface of the wafer before the CMOS circumvents the thermal problems, but introduces the challenge of overcoming the processing problems associated with surface topography.
- Interleaving various portions of the CMOS and MEMS processes enables tradeoffs to be made, but with a resulting system whose complexity and performance is limited by the required compromises.

# Integration Process Technology

- Still other approaches use materials for the mechanical structures other than polysilicon, such as stacked aluminium/silicon dioxide layers, for example.
- Clearly a method is needed that circumvents the problems associated with mechanical topography and high temperature anneals, while at the same time remaining fully compatible with conventional IC fabrication tools.
- Sandia's IMEMS technology does exactly that, enabling the highest performance electronics to be directly integrated with advanced polysilicon surface micromachined devices.

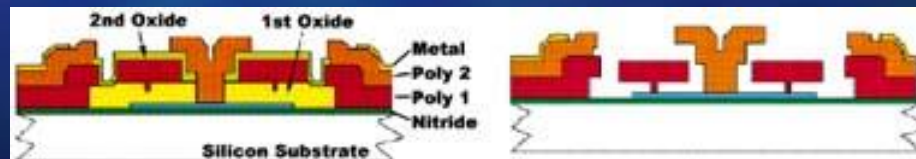


# IMEMS Process Technology

- The primary enabling aspect of Sandia's IMEMS technology is the formation of the mechanical devices in a trench prior to the fabrication of the associated CMOS circuitry.
- As illustrated in Figure 18, a 12 micron deep trench is first etched into the silicon substrate. Using special photolithography methods
- Surface micromachined polysilicon devices (similar to those made using the SUMMiT process) are formed in the trench.
- The trench is then filled with silicon dioxide, and then planarized even with the surface of the wafer using a process called Chemical-Mechanical Polishing, or CMP

# IMEMS Process Technology

- At this point, a perfectly planar wafer is ready to start CMOS processing, with the mechanical devices having already been created and annealed.
- At the end of the CMOS processing, electrical interconnections are made to the mechanical devices.
- Finally, the silicon dioxide encapsulating the mechanical devices in the trench is etched away, resulting in mechanical devices electrically interconnected to adjacent circuitry on the same chip.



## SNL Integrated Micromechanical / CMOS

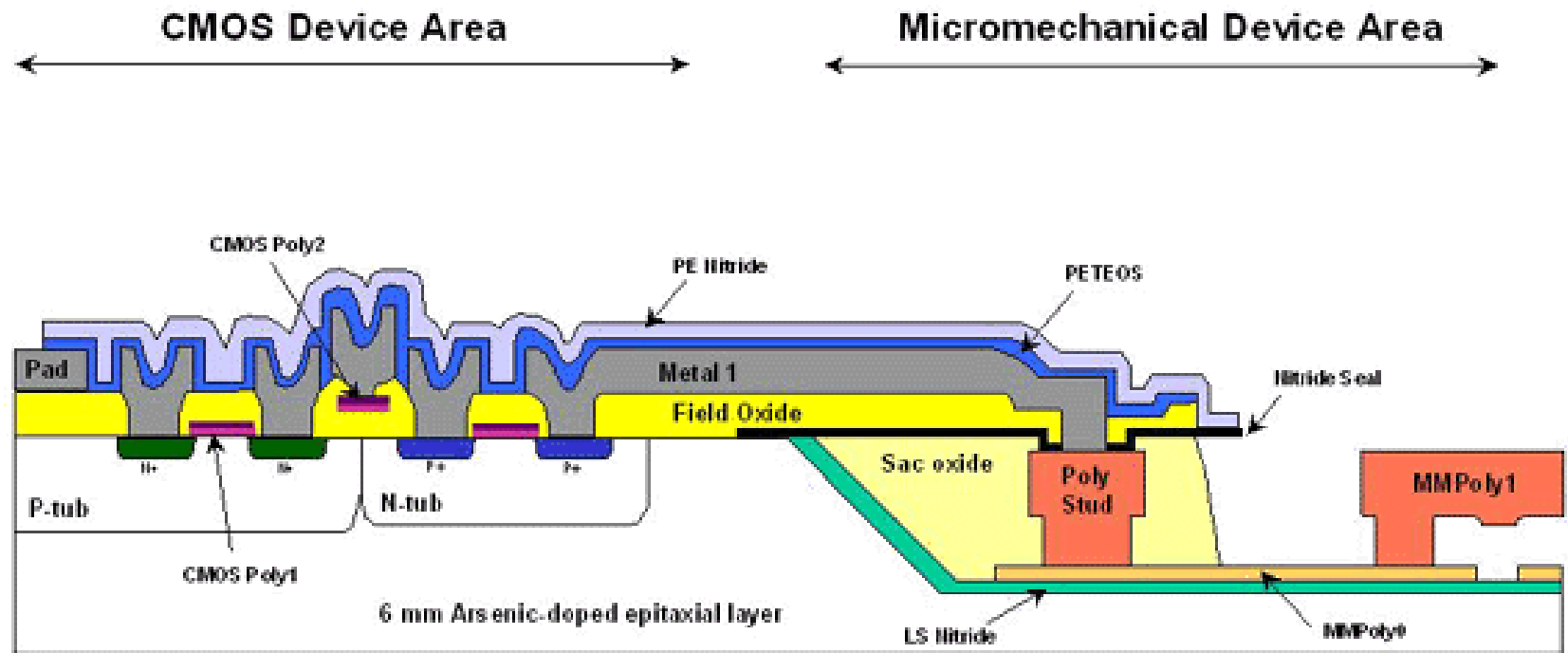


Figure 18. Cross-section schematic of trench integration



# Advantages

- The use of polysilicon as the structural material is advantageous because of its excellent mechanical properties.
- Since the MEMS elements are fabricated first, any high temperature anneals do not affect the CMOS circuitry.
- The process is completely modular; this enables the planarized wafers to be processed in any facility with virtually any IC process (e.g., CMOS, bipolar, etc.).

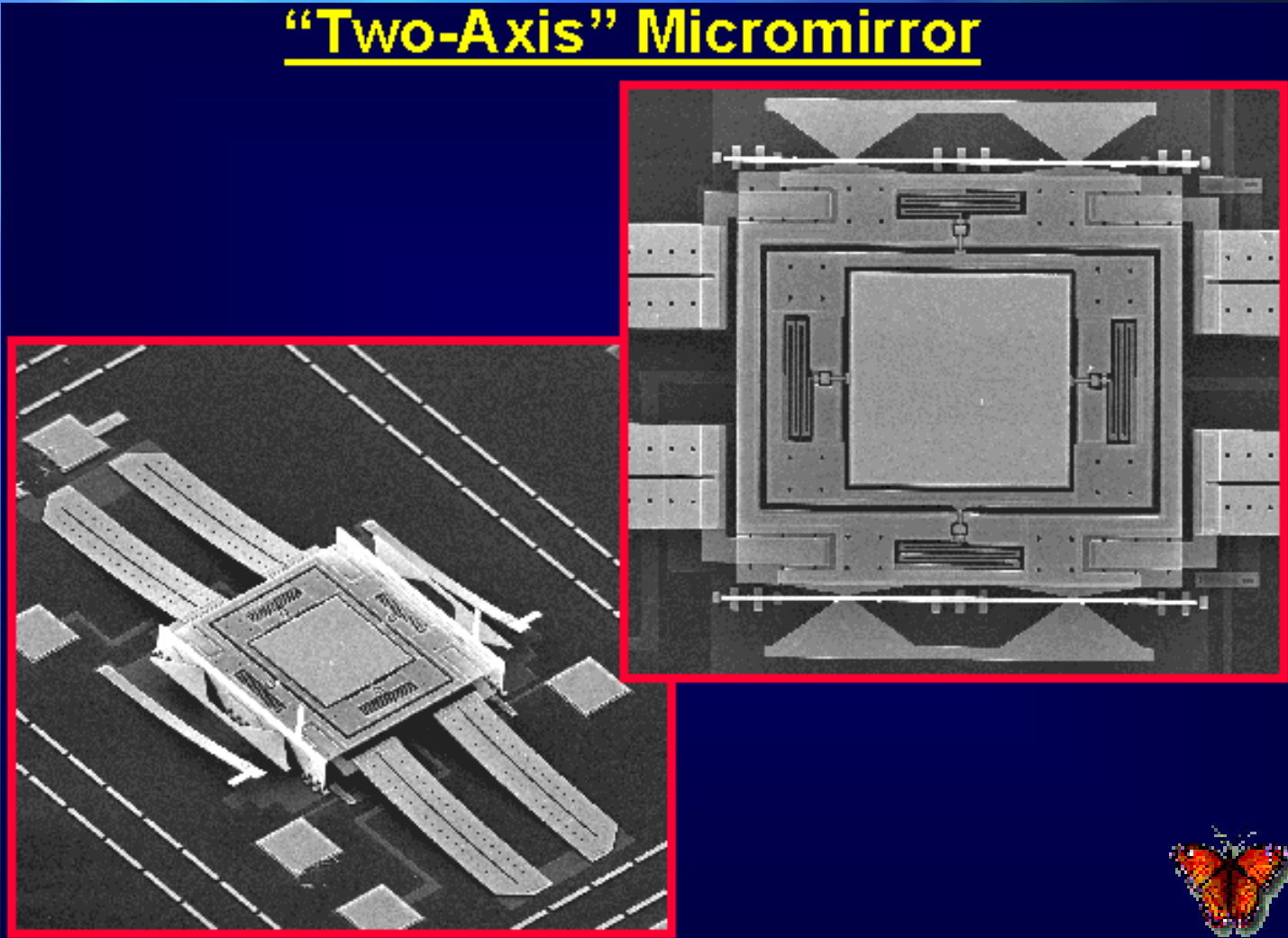
# Advantages

- Modularity also enables the mechanical devices and electronic circuitry to be independently optimised, making possible the development of very high-performance microsystems.
- Finally, the fabrication tools used in this process are common to the IC industry.
- For example, the CMP process is finding widespread application in many IC fabs that are processing sub-micron technologies.

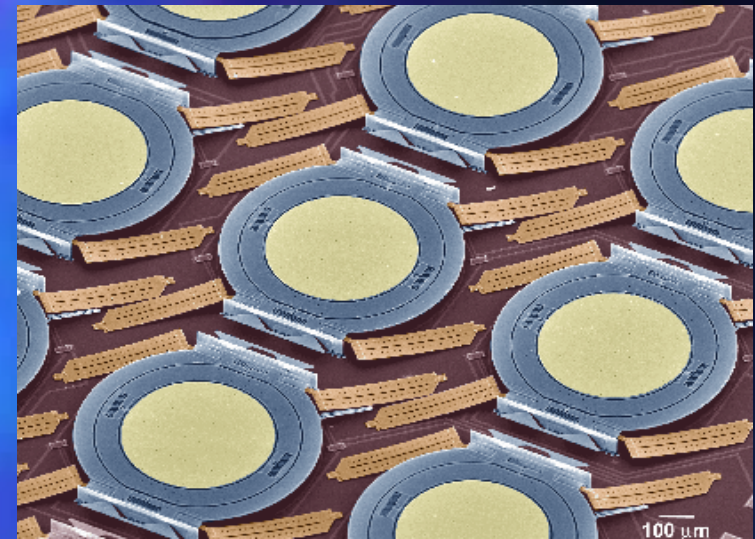
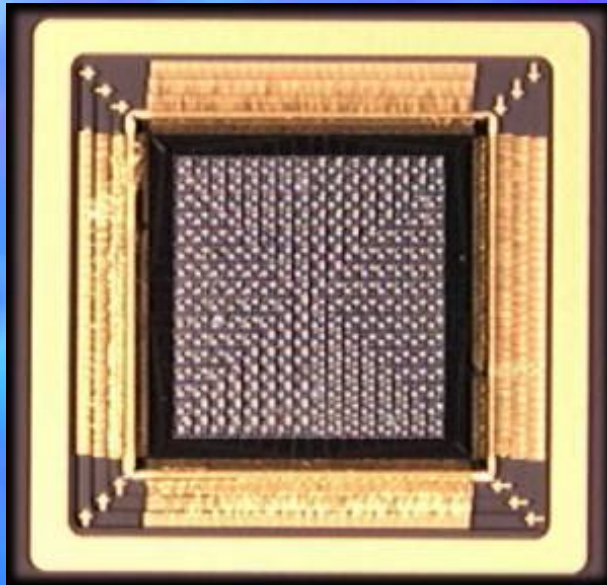


# Optical Switching Using MEMS Technology

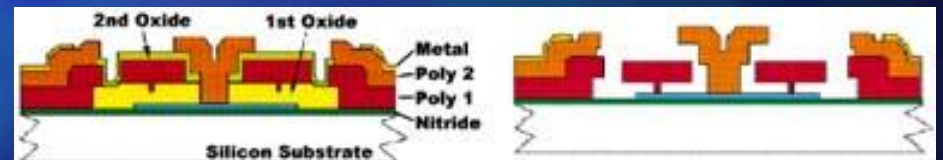
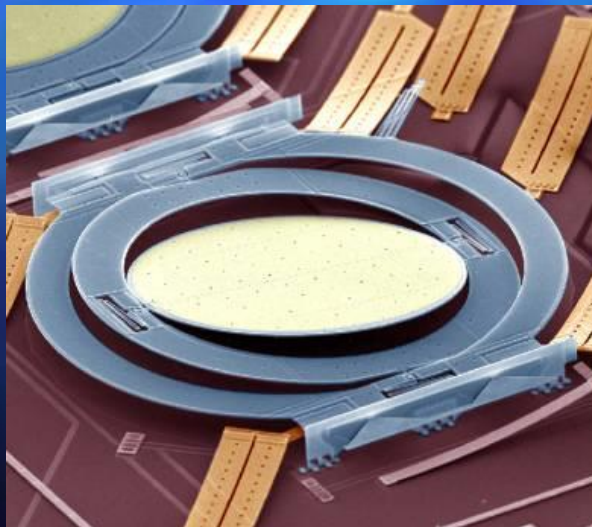
## "Two-Axis" Micromirror





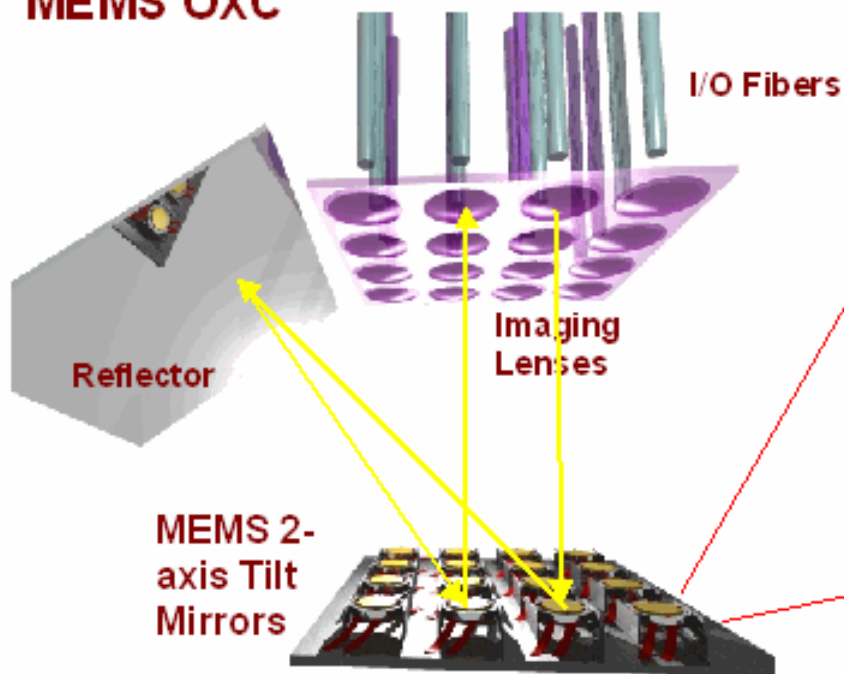


Packaged Microstar Mirror Array with 256 mirrors



# Lucent MEMS OXC

## **MEMS OXC**



### **MEMS DEVICE:**

- 2-axis, angular range of  $> \pm 6^\circ$
- continuous, controlled tilt
- directly scalable to 256 mirrors ( 1024 in the long term )
- simple technology for rapid development / prototyping
- manufacturable



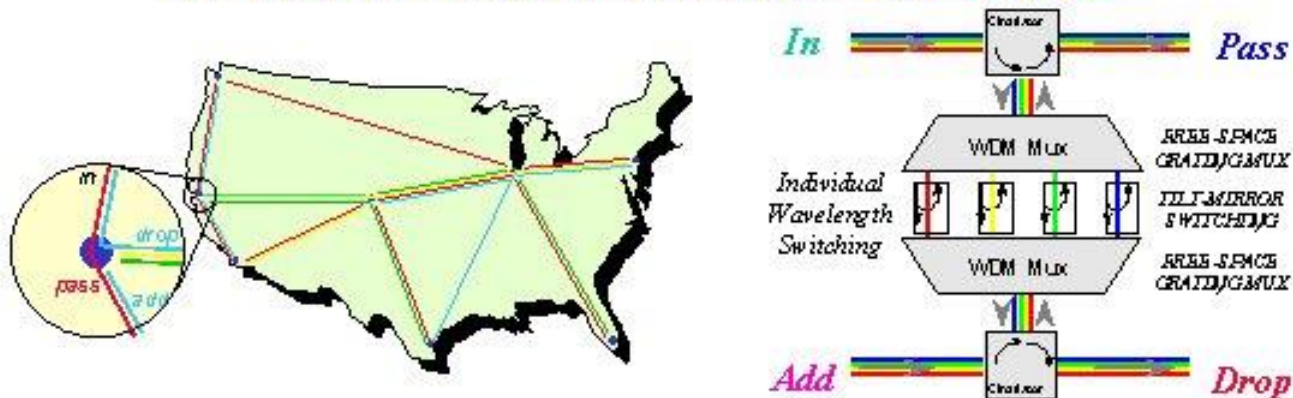
# Cross Connect Realisation





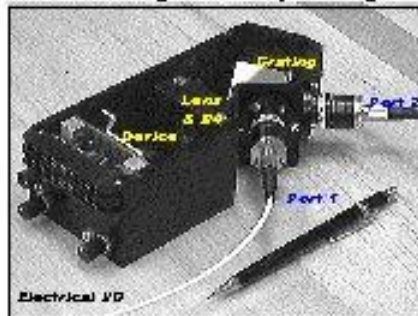
# Wavelength-Selectable Add/Drop

**Dynamic WDM network reconfiguration for SONET and Metropolitan WDM for efficient bandwidth allocation & fault recovery**

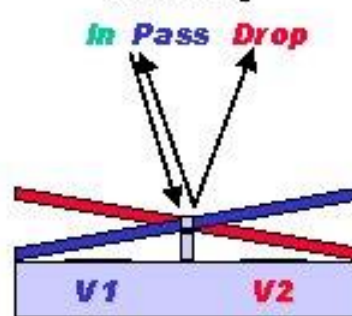


**Free-space wavelength multiplexing onto MEMS tilt-mirror switches**

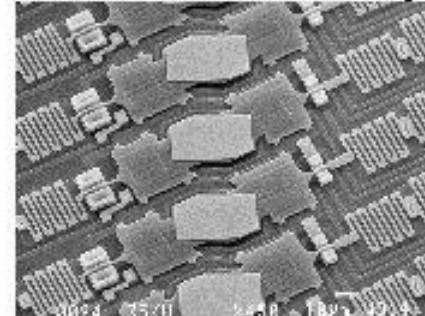
**Wavelength Multiplexing**



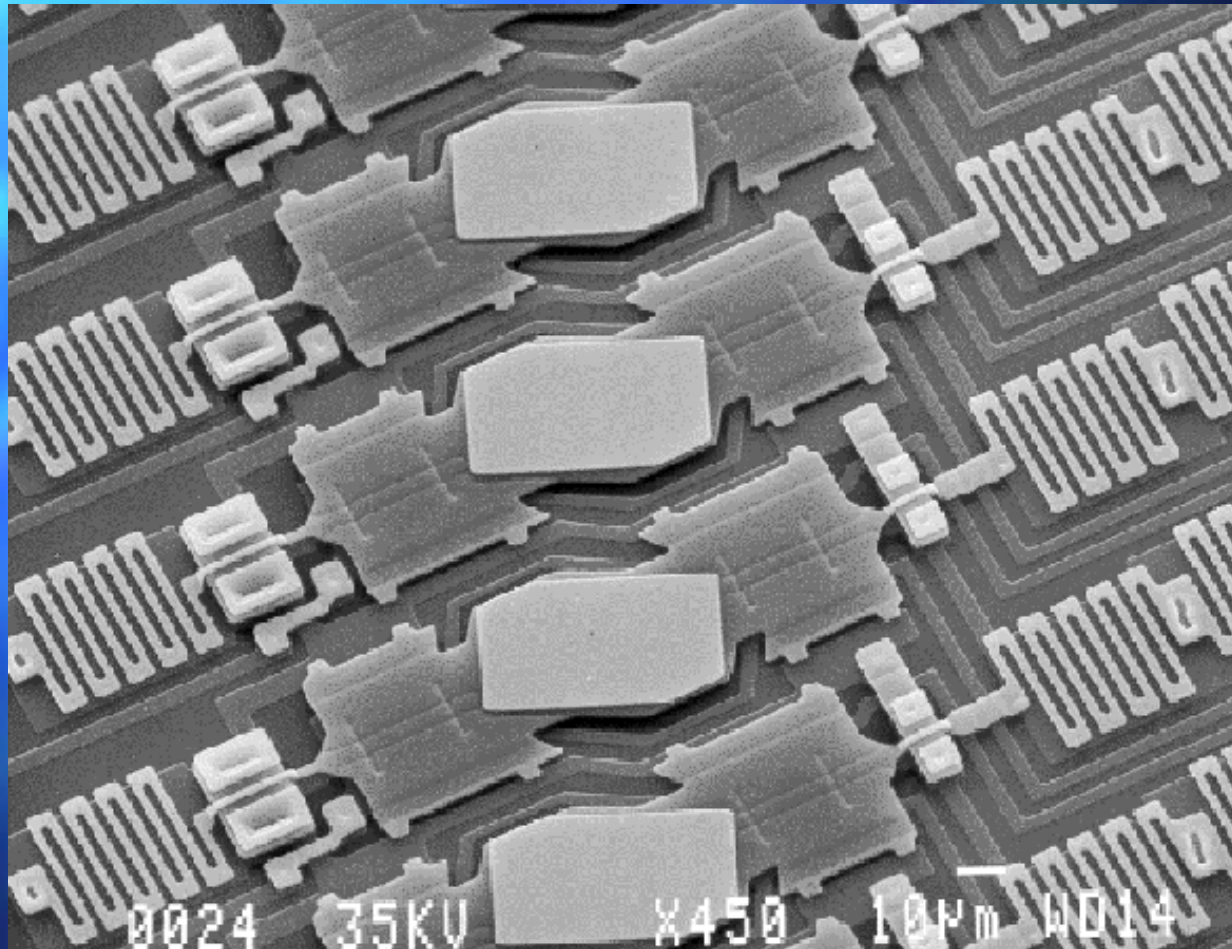
**Switching**



**16 Channel Tilt-Mirror Array**



# Add/Drop Multiplexer

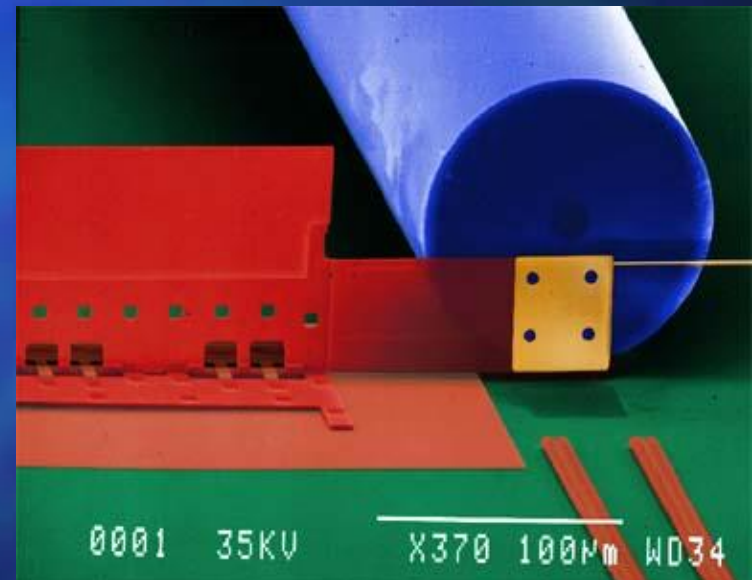






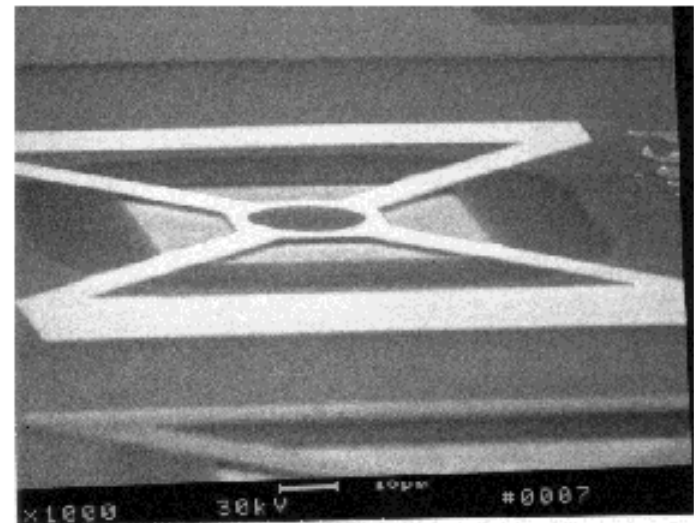
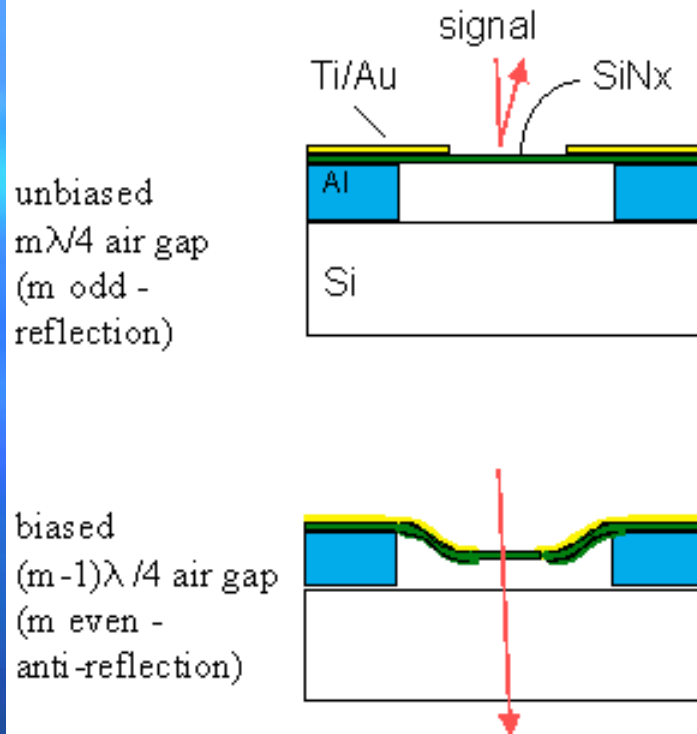
**MEMS optical switch can route from the input fibre to one of the two output fibres**

**Self assembly techniques allow the hinged plate with the mirror to stand on its own during the release step**



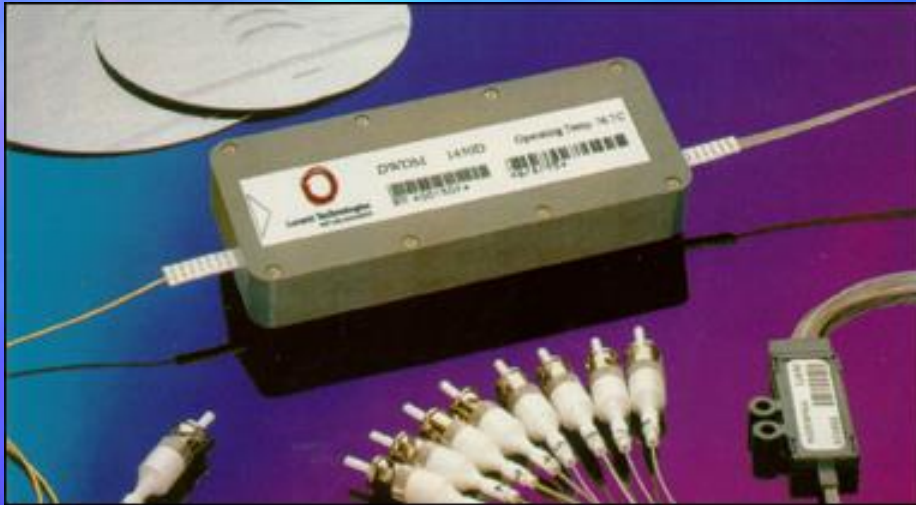


## MARS - Mechanical Anti-Reflection Switch



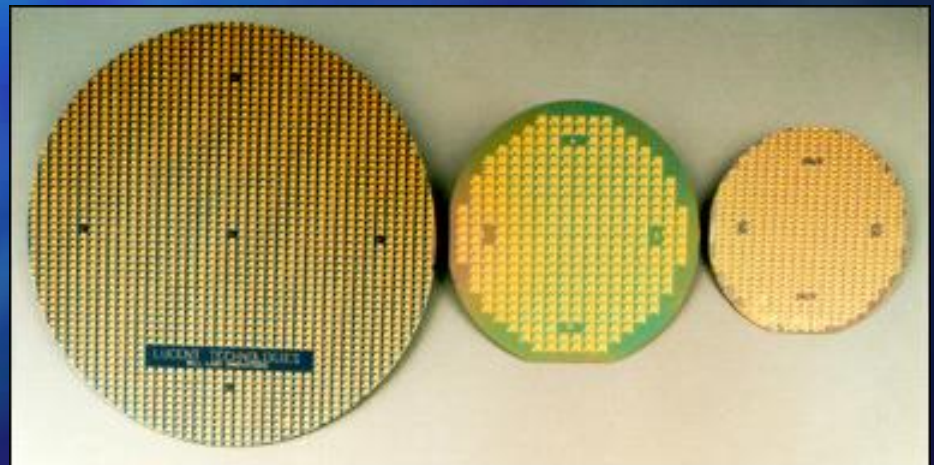
Fully fabricated MARS device

# Silicon Optical Bench (SiOB) Technology

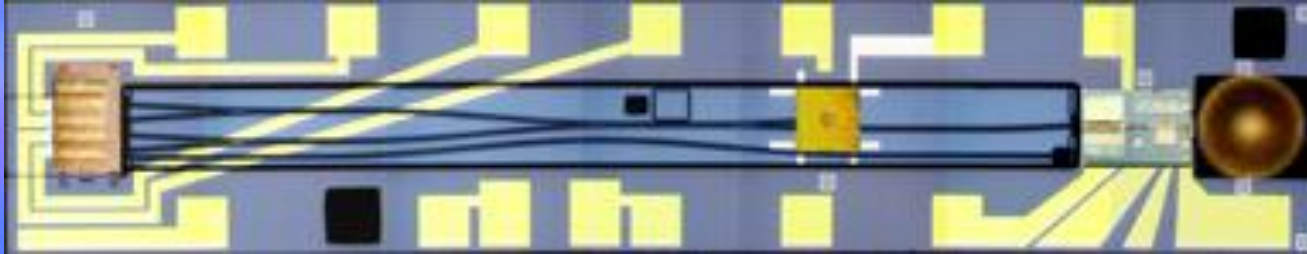


**Silicon Optical Bench (SiOB) technology is a fabrication platform for integrated optical device components. This technology will find applications in optical networks, especially those where wavelength division multiplexing (WDM) is employed.**

**SiOB technology uses silicon wafers as a platform to fabricate passive and active integrated optical circuits. The formation of these circuits involves the deposition and patterning of oxides, patterning and deposition of metals and solders, and deep anisotropic etching of the silicon for fibre and ball lens alignment**



# Silicon Optical Bench (SiOB) Technology

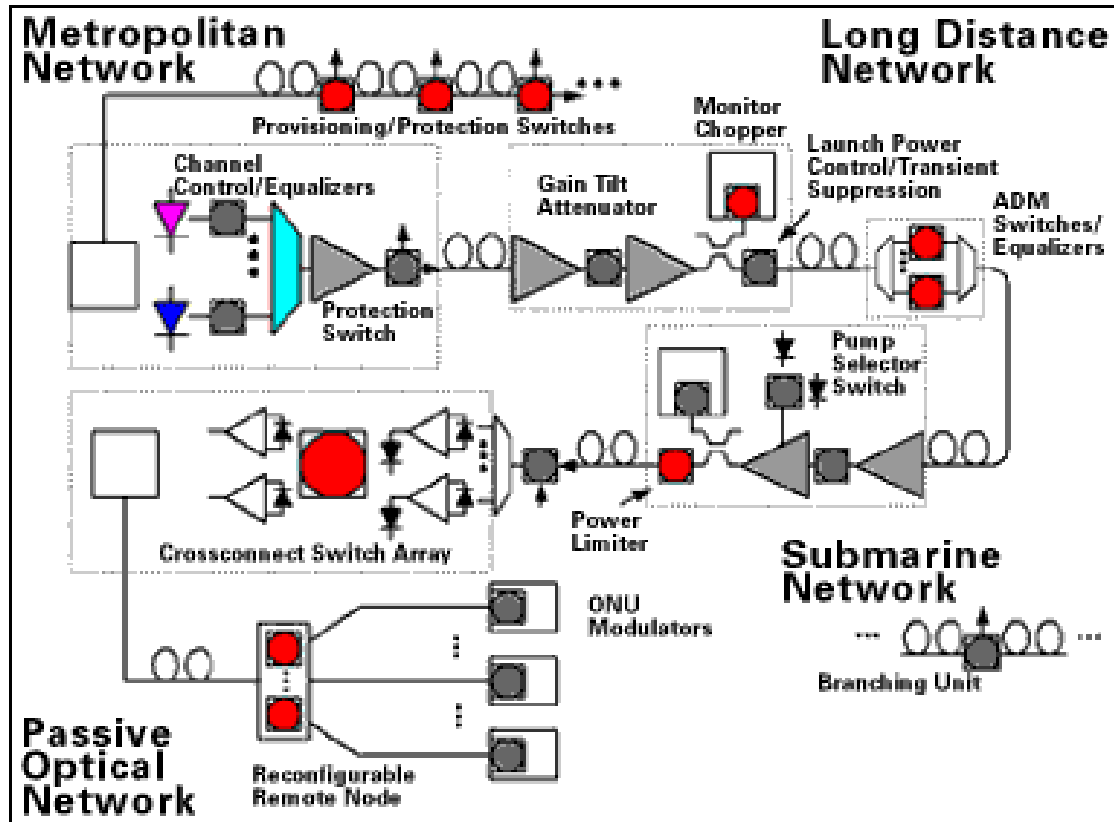


The example above demonstrates the use of the SiOB technology to form an integrated transceiver chip. In a fibre-to-the-home system, the transceiver would sit on the side of the home and provide the optical-to-electrical conversion, it operates at 150Mb/s



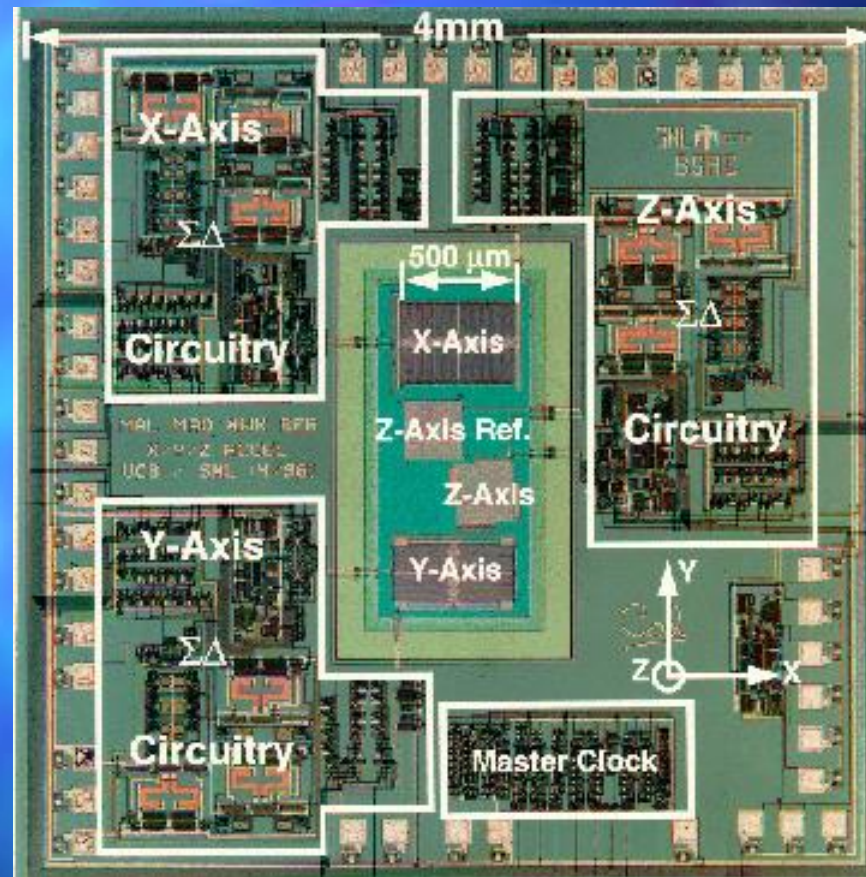
Packaged transceiver chip, can also be used to produce multiple wavelength sources, reconfigurable add/drop multiplexers, above right.





# Example Device

- A three-axis, force-balanced accelerometer designed by engineers from the Berkeley Sensor and Actuator Centre (BSAC) at U.C. Berkeley is shown in Figure 19.
- This three-axis accelerometer system-on-a-chip exhibits an order of magnitude increase in sensitivity over the best commercially available single-axis MEMS device.
- The Berkeley design also includes clock generation circuitry, a digital output, and photolithographic alignment of the sense axes.
- Thus, this system-on-a-chip is a realization of a full three-axis inertial measurement unit that does not require manual assembly and alignment of sense axes.



**Figure 19. Three-axis accelerometer micrograph with labelling of functional units as reported by Lemkin et al, Proc. ISSCC '97.**



# Navigation System

- A long-term goal of a micromachined micro-navigation system requires both 3-axis accelerometers and gyroscopes.
- A combined X/Y-axis rate gyro and a Z-axis rate gyro have also been designed by researchers at U.C. Berkeley and have been fabricated in the IMEMS technology to yield a full six-axis inertial measurement unit on a single chip.
- The 4 mm by 10 mm system is manufactured on the same silicon substrate as the 3-axis accelerometer and will form the heart of a future micro-navigation system.

# Navigation System



- The objective of this project is to fabricate surface micromachined MEMS modules with state-of-the-art standard electronics.
- This capability will be demonstrated with a monolithic six-degrees-of-freedom inertial measurement unit.
- The approach involves increasing the thickness of the mechanical polysilicon structures from two microns to six microns, and the devices manufactured thus far have been demonstrated to be significantly more sensitive and robust.

# Smart Dust

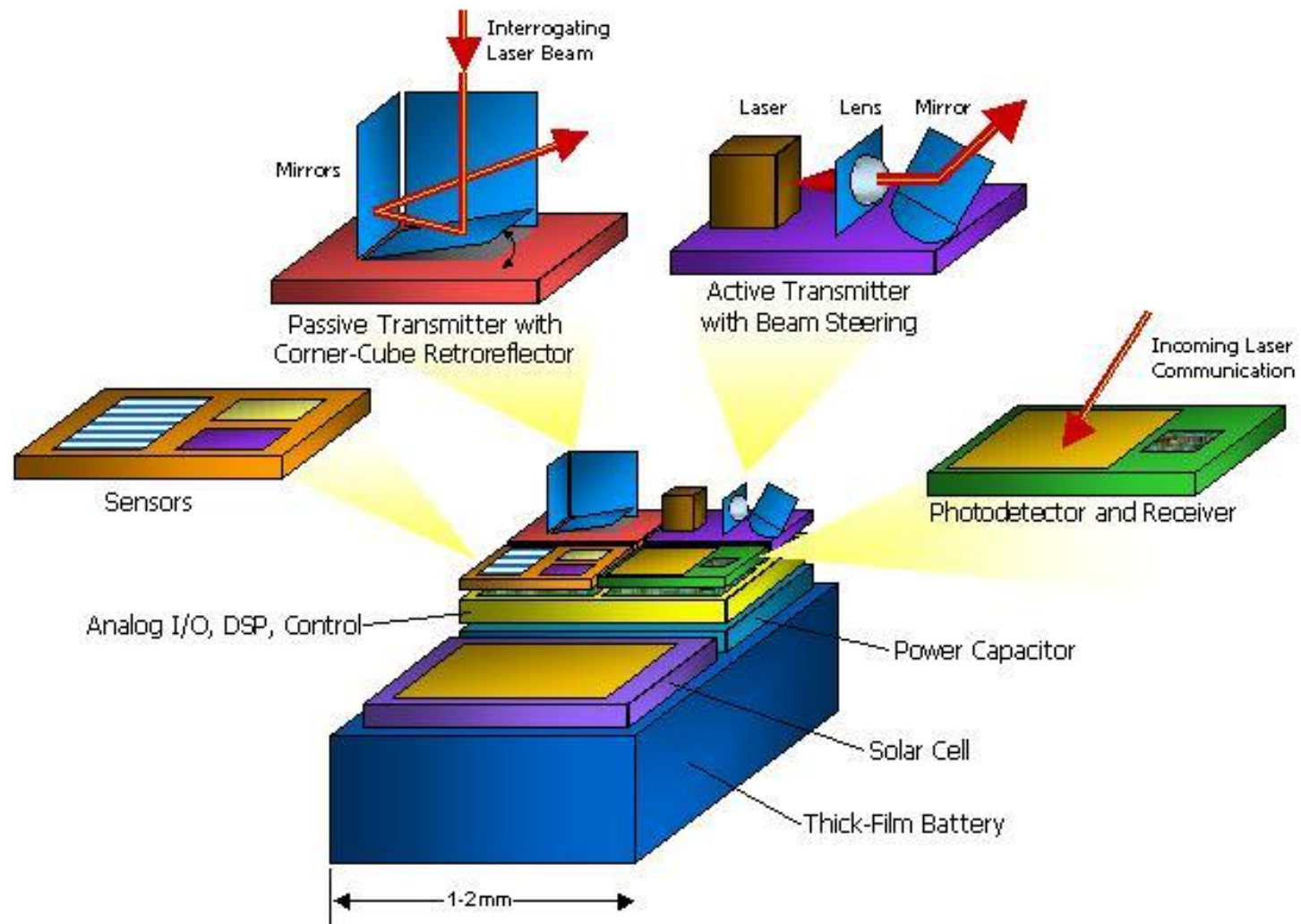
- The goal of the Smart Dust is to build a self-contained, millimeter-scale sensing and communication platform for a massively distributed sensor network.
- This device will be around the size of a grain of sand and will contain sensors, computational ability, bi-directional wireless communications, and a power supply, while being inexpensive enough to deploy by the hundreds.
- The science and engineering goal of the project is to build a complete, complex system in a tiny volume using state-of-the-art technologies
- As opposed to futuristic technologies, which will require evolutionary and revolutionary advances in integration, miniaturization, and energy management.
- <http://robotics.eecs.berkeley.edu/~pister/SmartDust/>



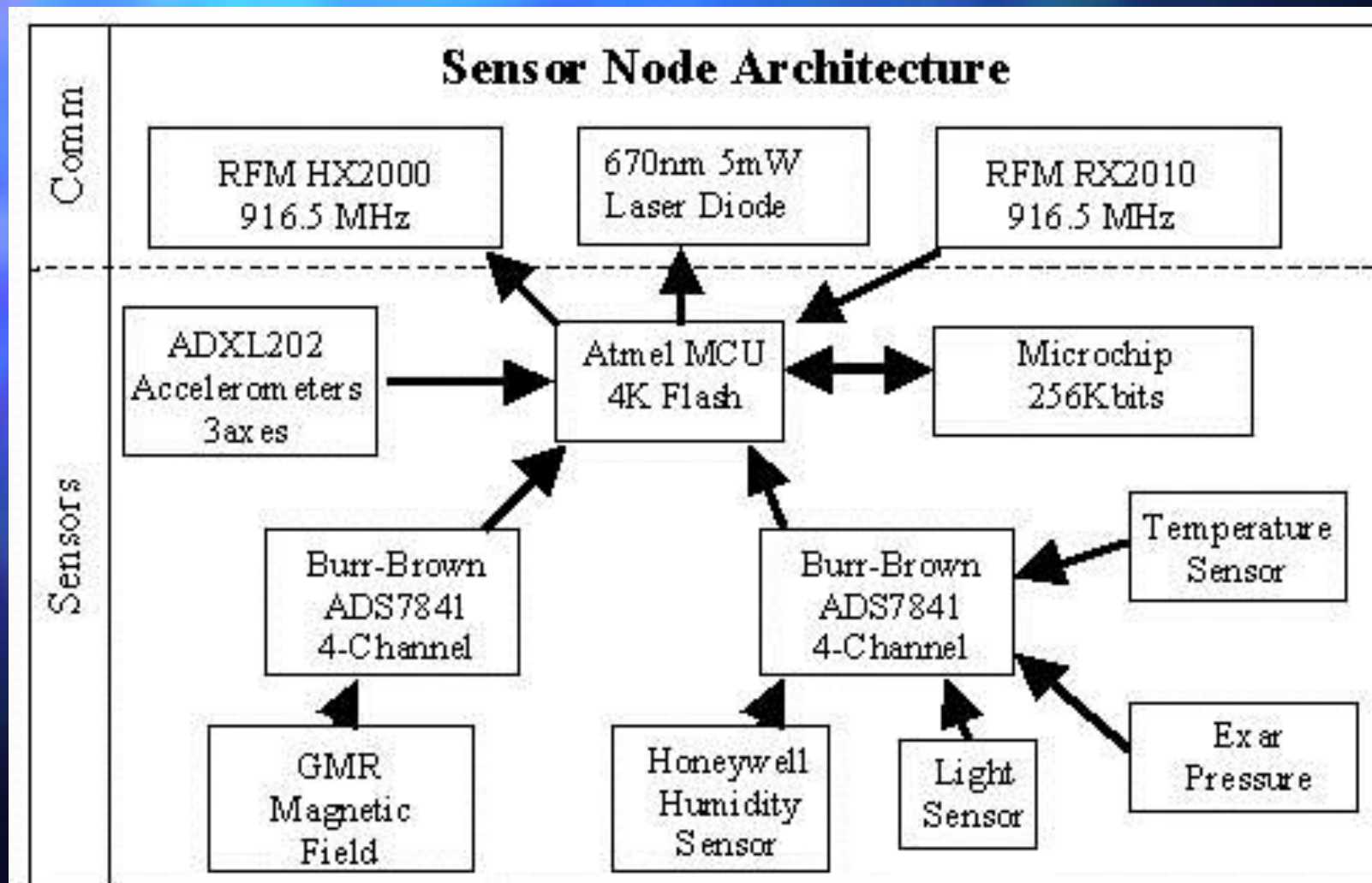
# Smart Dust

- There are many applications for this technology:
  - Weather/seismological monitoring on Mars
  - Internal spacecraft monitoring
  - Land/space comm. networks
  - Chemical/biological sensors
  - Weapons stockpile monitoring
  - Defence-related sensor networks
  - Inventory Control
  - Product quality monitoring
  - Smart office spaces
  - Sports - sailing, balls

# Smart Dust



# Sensor Node Architecture





# Mote Operation

- The primary constraint in the design of the Smart Dust motes is volume, which in turn puts a severe constraint on energy since we do not have much room for batteries or large solar cells.
- Thus, the motes must operate efficiently and conserve energy whenever possible. Most of the time, the majority of the mote is powered off with only a clock and a few timers running.
- When a timer expires, it powers up a part of the mote to carry out a job, then powers off. A few of the timers control the sensors that measure one of a number of physical or chemical stimuli such as temperature, ambient light, vibration, acceleration, or air pressure.
- When one of these timers expires, it powers up the corresponding sensor, takes a sample, and converts it to a digital word. If the data is interesting, it may either be stored directly in the SRAM or the microcontroller is powered up to perform more complex operations with it.
- When this task is complete, everything is again powered down and the timer begins counting again.

# Mote Operation

- Another timer controls the receiver. When that timer expires, the receiver powers up and looks for an incoming packet. If it doesn't see one after a certain length of time, it is powered down again.
- The mote can receive several types of packets, including ones that are new program code that is stored in the program memory. This allows the user to change the behavior of the mote remotely.
- Packets may also include messages from the base station or other motes. When one of these is received, the microcontroller is powered up and used to interpret the contents of the message.
- The message may tell the mote to do something in particular, or it may be a message that is just being passed from one mote to another on its way to a particular destination.

# Mote Operation

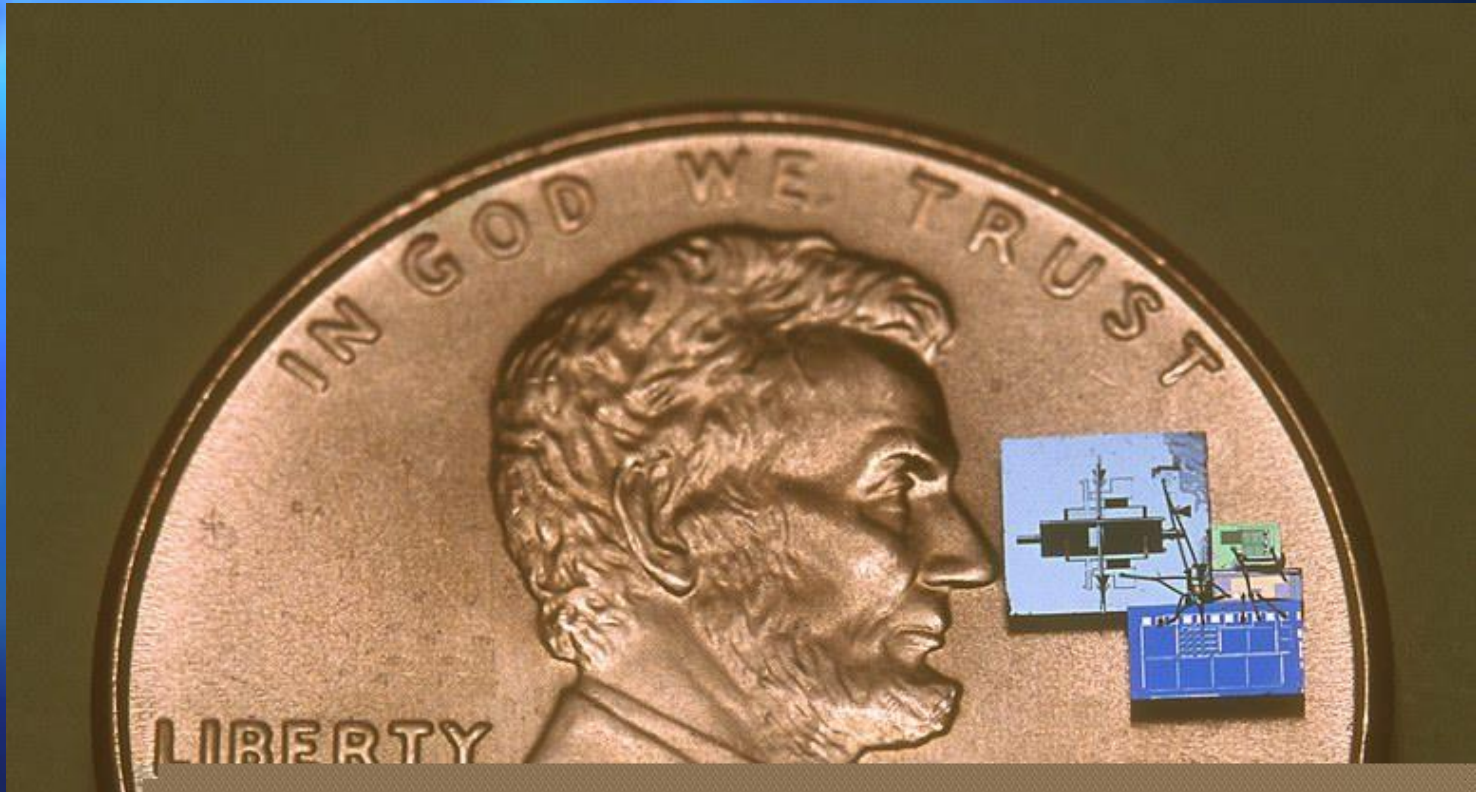
- In response to a message or to another timer expiring, the microcontroller will assemble a packet containing sensor data or a message and transmit it using either the corner cube retroreflector or the laser diode, depending on which it has.
- The corner cube retroreflector transmits information just by moving a mirror and thus changing the reflection of a laser beam from the base station.
- This technique is substantially more energy efficient than actually generating some radiation.
- With the laser diode and a set of beam scanning mirrors, we can transmit data in any direction desired, allowing the mote to communicate with other Smart Dust motes.



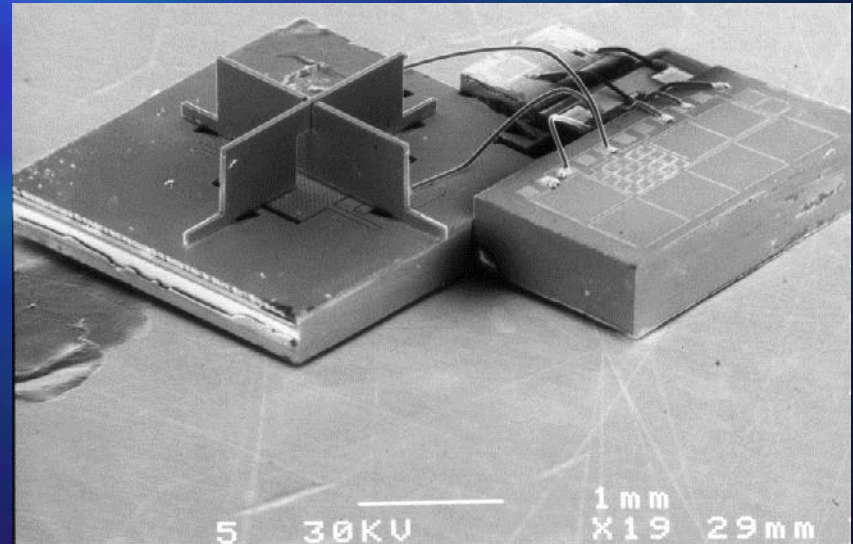
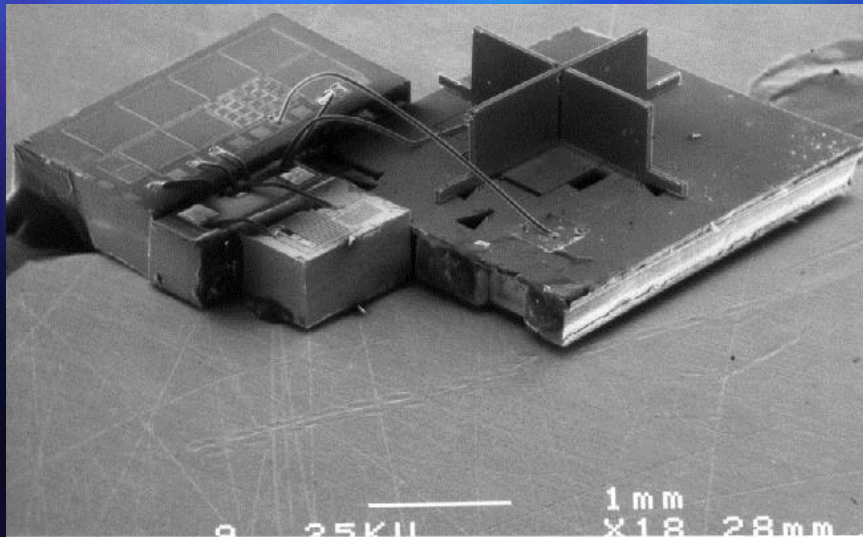
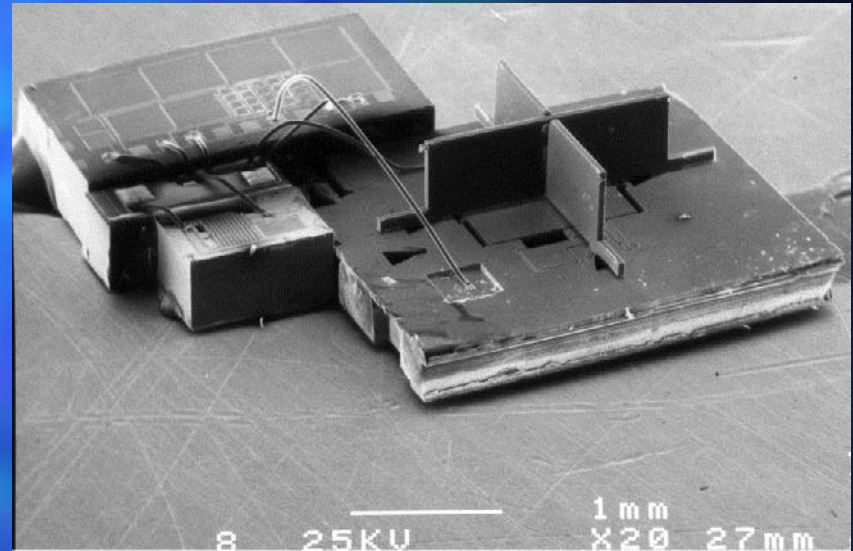
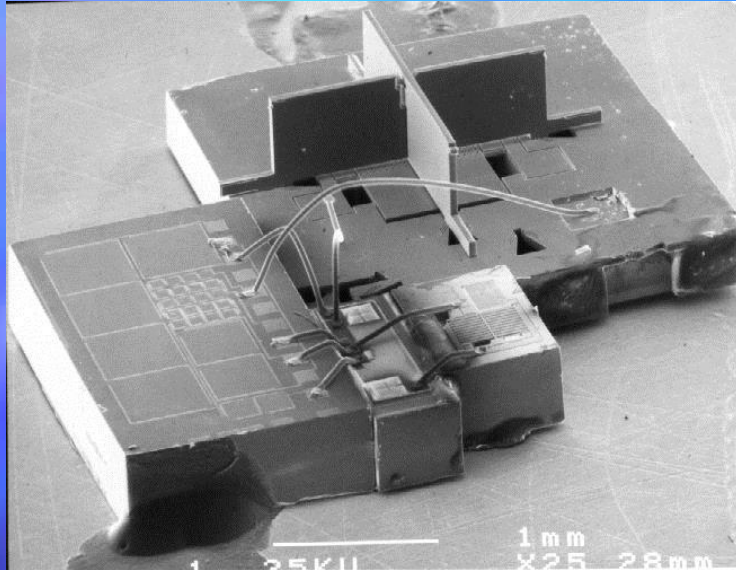
## Golem Dust

*solar powered mote with bi-directional communications and sensing  
(acceleration and ambient light)*

*11.7 mm<sup>3</sup> total circumscribed volume ~4.8 mm<sup>3</sup> total displaced  
volume*

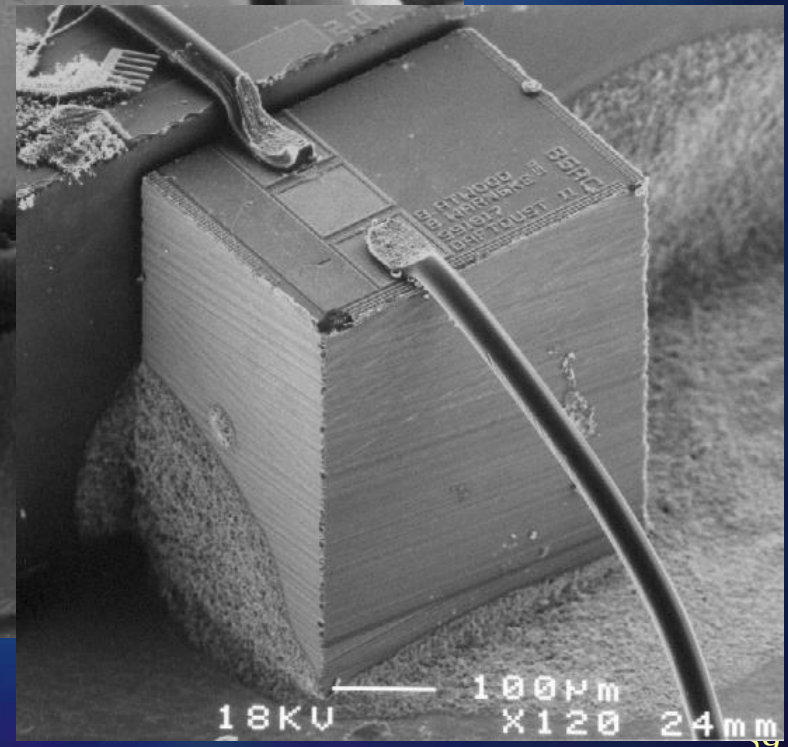
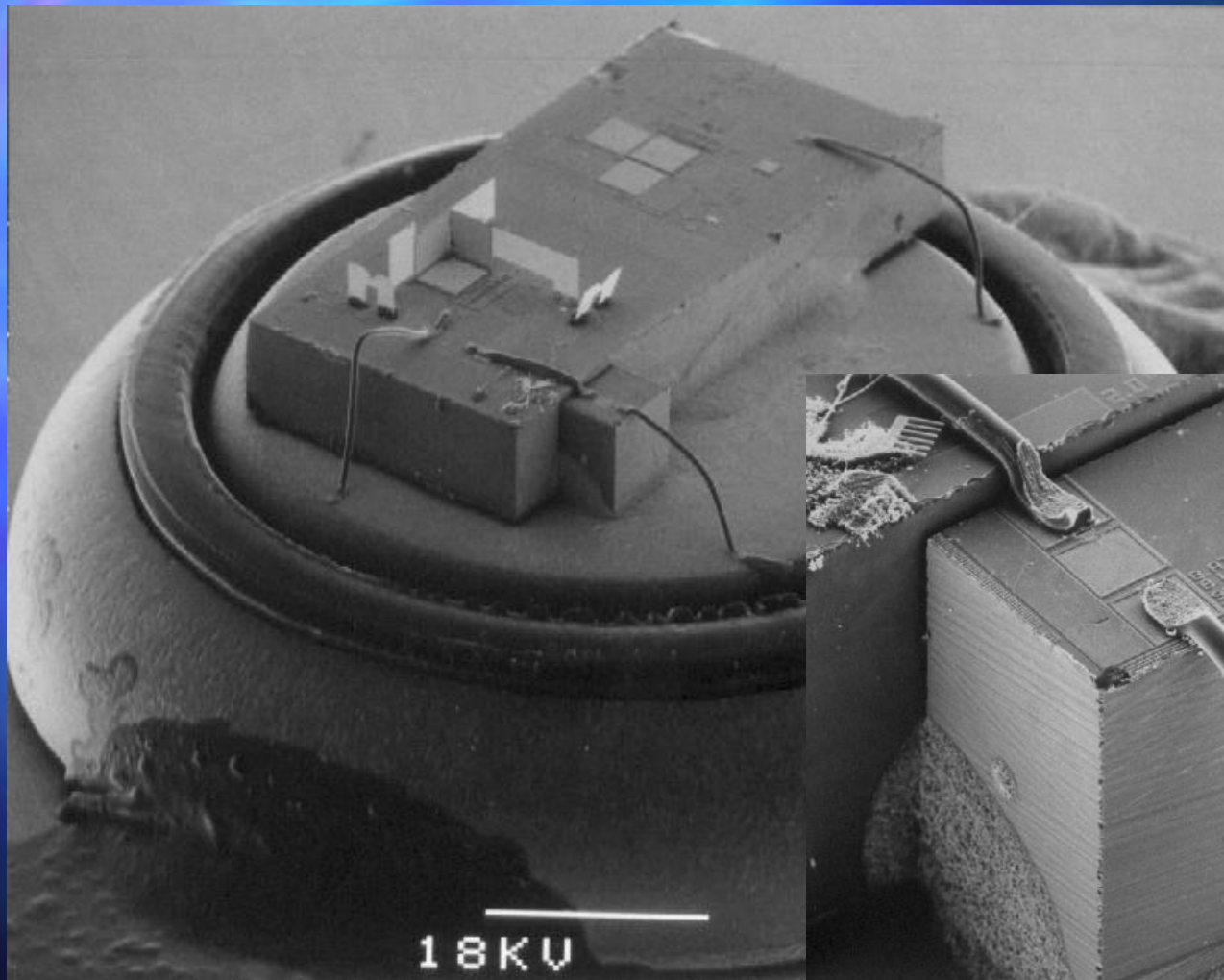


# Golem Dust



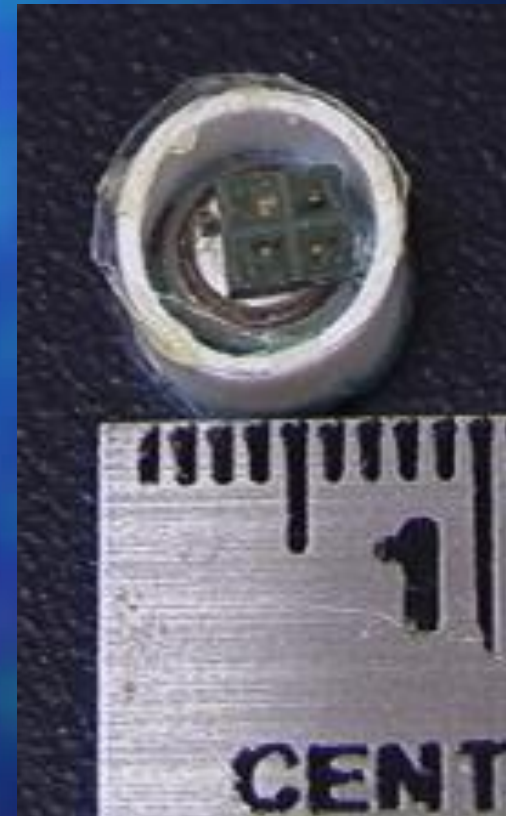
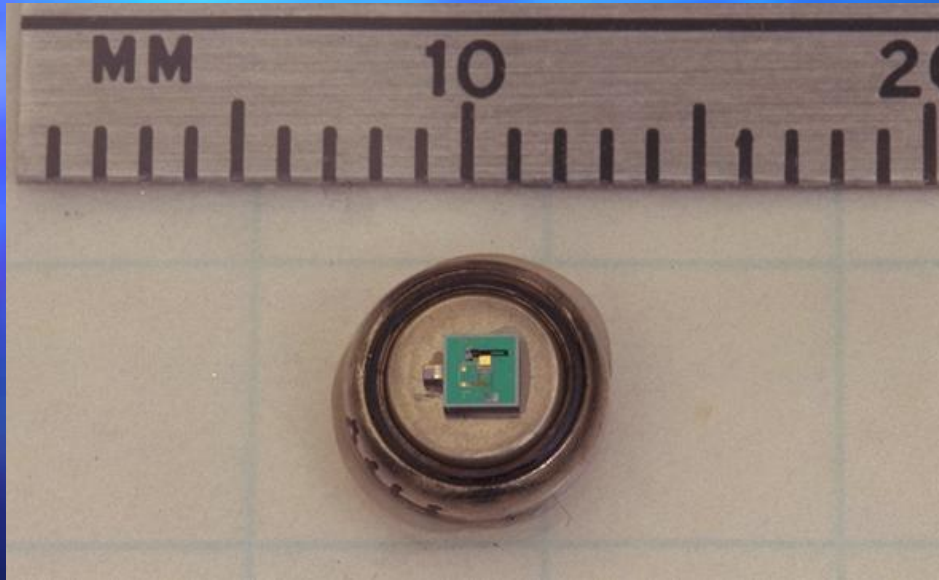


Daft Dust  
*63 mm<sup>3</sup> bi-directional communication mote*



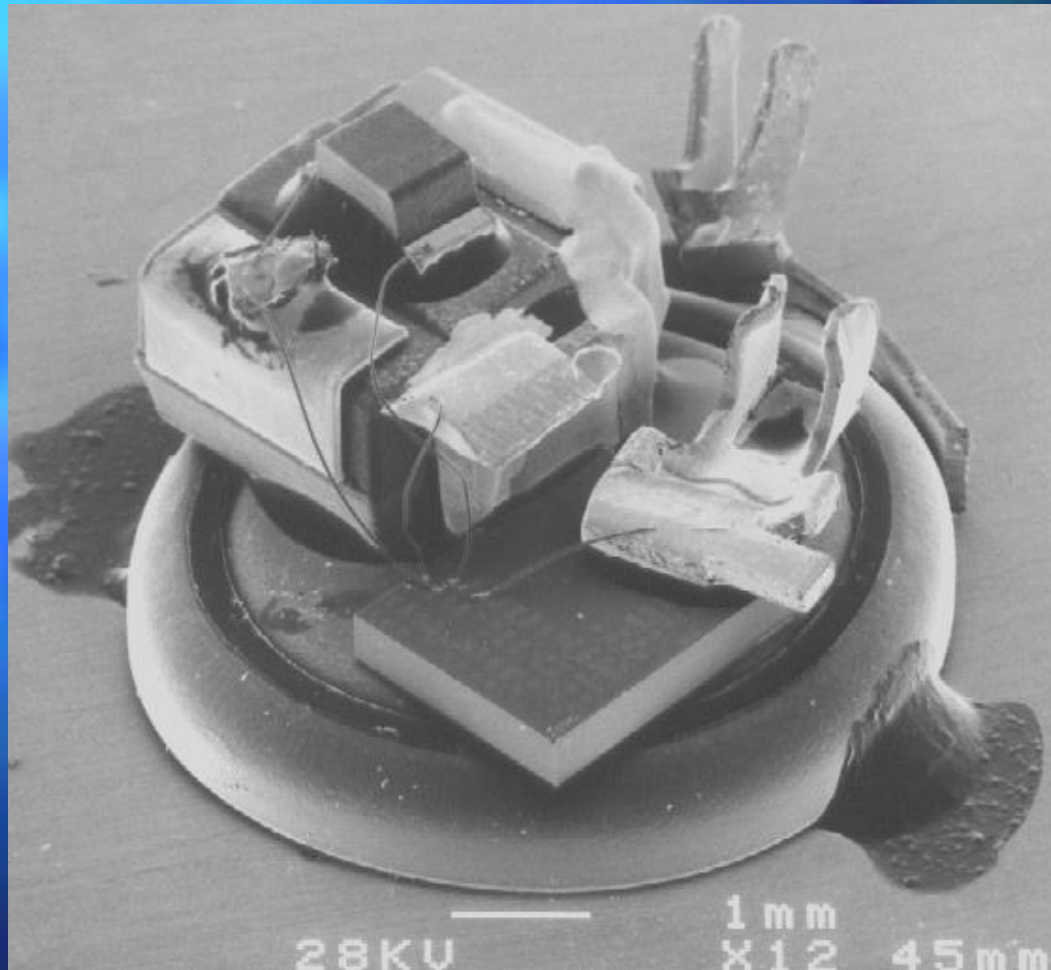


This mote has four CCR's facing towards each quadrant for better hemispherical coverage



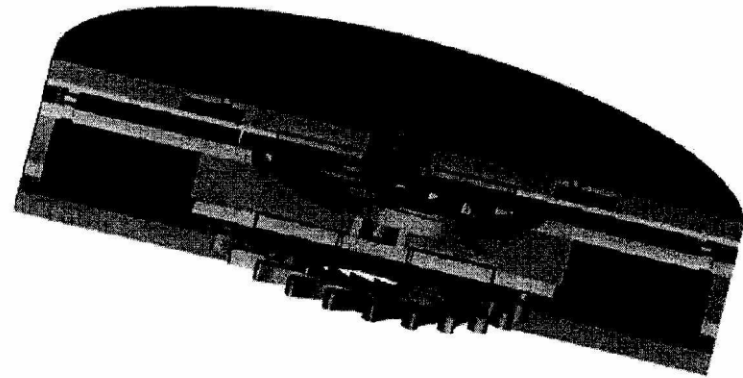
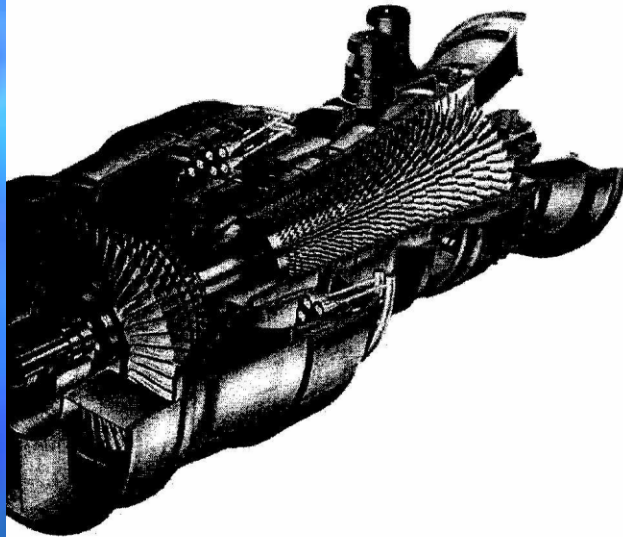
## Flashy Dust

*138 mm<sup>3</sup> uni-directional communication and sensing (ambient light) mote*



# MIT Micro Gas Turbine Generator

## MIT Micro Gas Turbine Generator

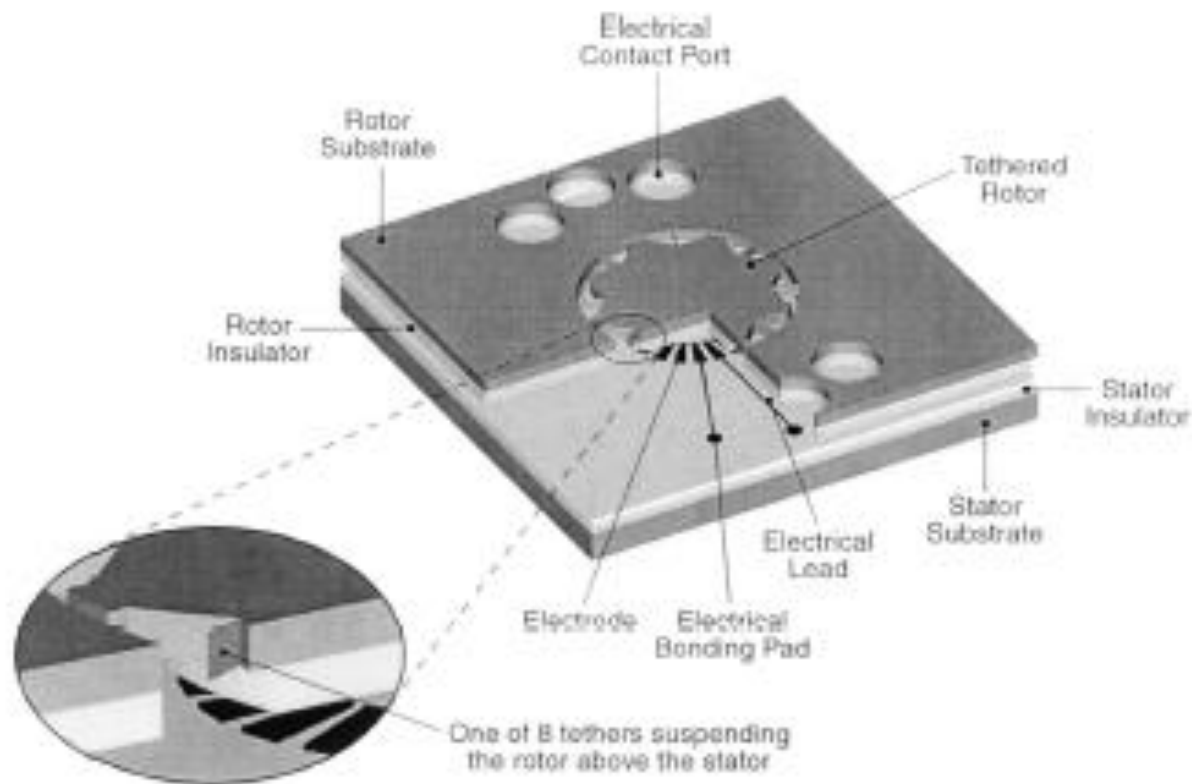


	Micro Turbo Generator	LiSO2 Battery (BA5590)
Power Output	50 W	50 W
Weight	50 grams	1000 grams
Specific Energy	3500 W-hr/kg	175 W-hr/kg

- A portable power source with ten times the power density of state-of-art batteries



# Micro Magnetic Machines for Micro Turbomachinery



*Fig. 11: Perspective view of the tethered electric induction motor.*

# Micro Magnetic Machines for Micro Turbomachinery

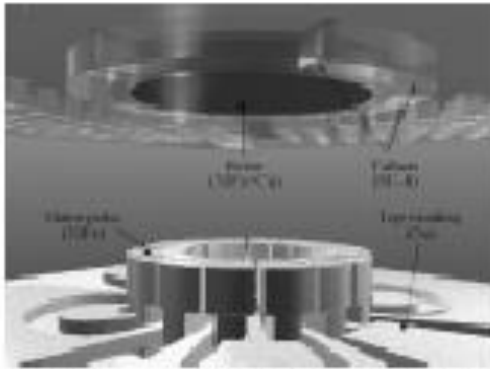
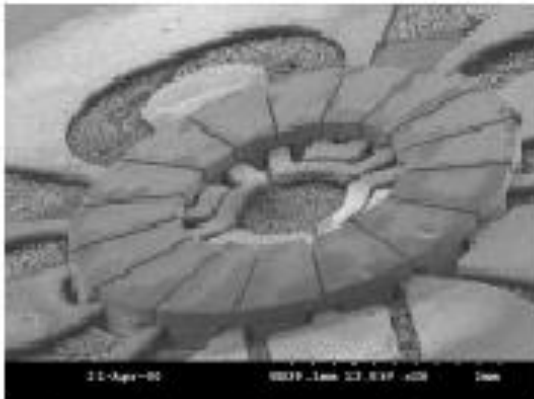


Fig. 30: An expanded view of a tethered micro magnetic induction



motor showing the rotor above and the stator below.

Fig. 31: A micrograph of an experimental stator after the insulation has been etched away to reveal the top phase of the stator windings. The outer radius of the stator core is 2 mm.

Test results so far have demonstrated that the motors can be successfully run at their rated currents of 13 A peak per phase. This corresponds to a current density of  $109 \text{ A/m}^2$

An expanded drawing of an electroplated tethered motor is shown in Figure 30.

The upper half of the figure shows a copper conducting film deposited on a nickel-iron rotor suspended by epoxy or Kapton tethers.

The lower half of the figure shows the stator comprises a nickel-iron core and two copper windings that pass in quadrature through slots in the core; each winding occupies a separate layer.

# MIT Micro-turbomachinery

Recent advances in silicon microfabrication technology have led to the realization of miniature heat engines for portable power generation and micro air vehicle propulsion.

As part of a program to develop a button-sized micro gas turbine engine capable of providing 10-50 Watts of electrical power in a 1cm<sup>3</sup> package, MIT have completed the design, fabrication and initial testing of the first engine staticstructure micromachined from silicon.

Comprising all the non-rotating functional components of a Brayton-cycle based gas turbine engine, the device measures 2.1 cm · 2.1 cm · 0.38 cm, and is aligned-fusion bonded from 6 silicon wafers.

As shown in Figure 12, this static structure is the first demonstration of the entire hot flow path of a 6-wafer multi-level microengine, and is fully-compatible with the thermal, structural and fabrication constraints of the final engine configuration.



# MIT Microturbomachinery

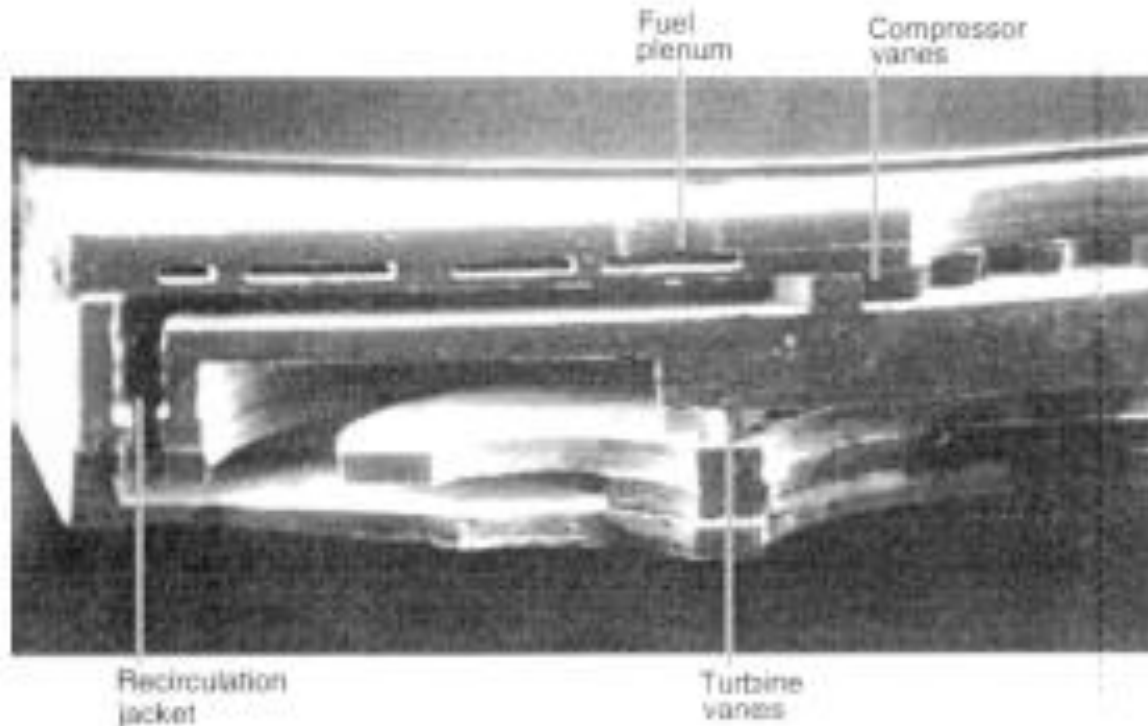
Fabricated largely through the use of Deep Reactive Ion Etching (DRIE), the structure required anisotropic dry etching through a total thickness of 3,800  $\mu\text{m}$ .

Complete with a set of fuel plenums, fuel injector holes, pressure ports and compressor and turbine static blades, the design of the static structure required a multi-disciplinary approach that accounted for all the chemical, structural, fluidic, and materials fabrication aspects of the engine.

For the propulsion and power generation applications of interest, the principal figure of merit for the propulsion system is the power density.

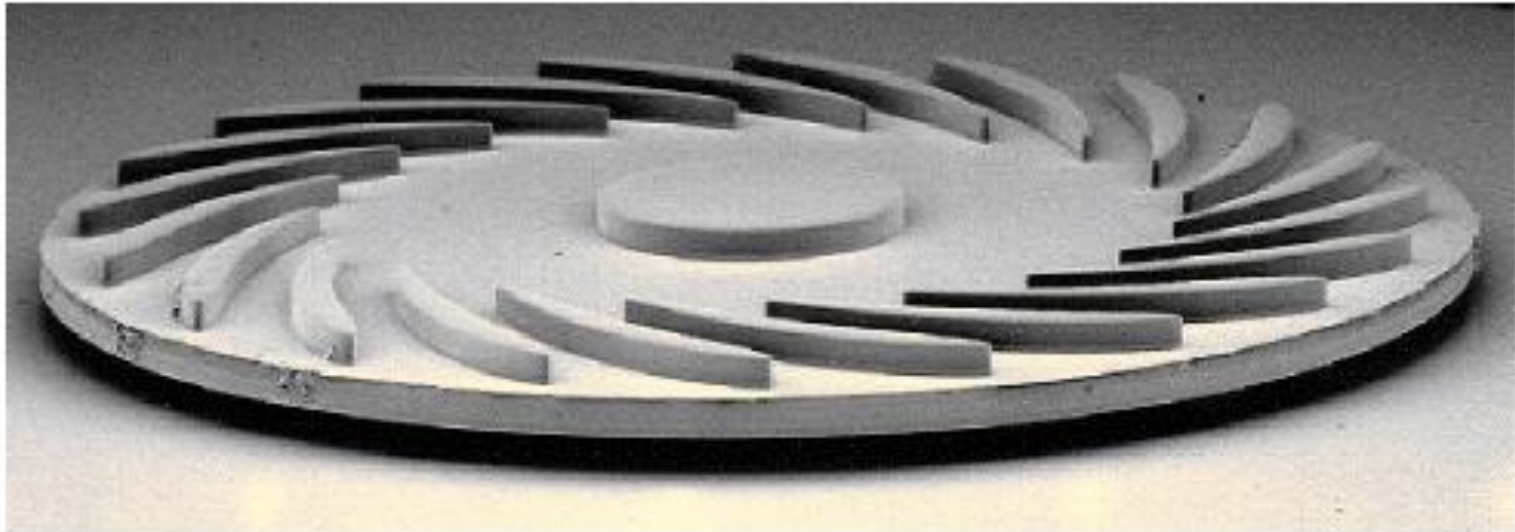
The device has been shown to sustain hydrogen-air combustion in a chamber measuring 0.195  $\text{cm}^3$  in volume with exit gas temperatures as high as 1725K. The resulting power density of the combustion system is at least an order of magnitude higher than any other previously reported power-MEMS device.

# MIT Micro-turbomachinery



*Fig. 12: Schematic and SEM cross-section of half of the axisymmetric 6-wafer static structure.*

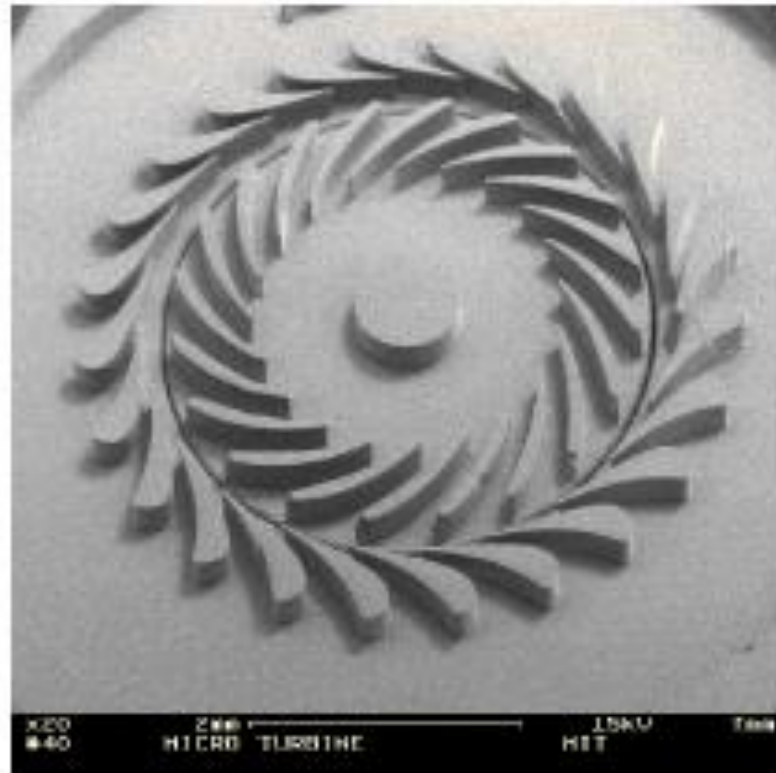
# MIT Micro-turbomachinery



*Fig. 14: Free standing SiC microengine rotor created by CVD into an Si mold. The rotor diameter is 4 mm*

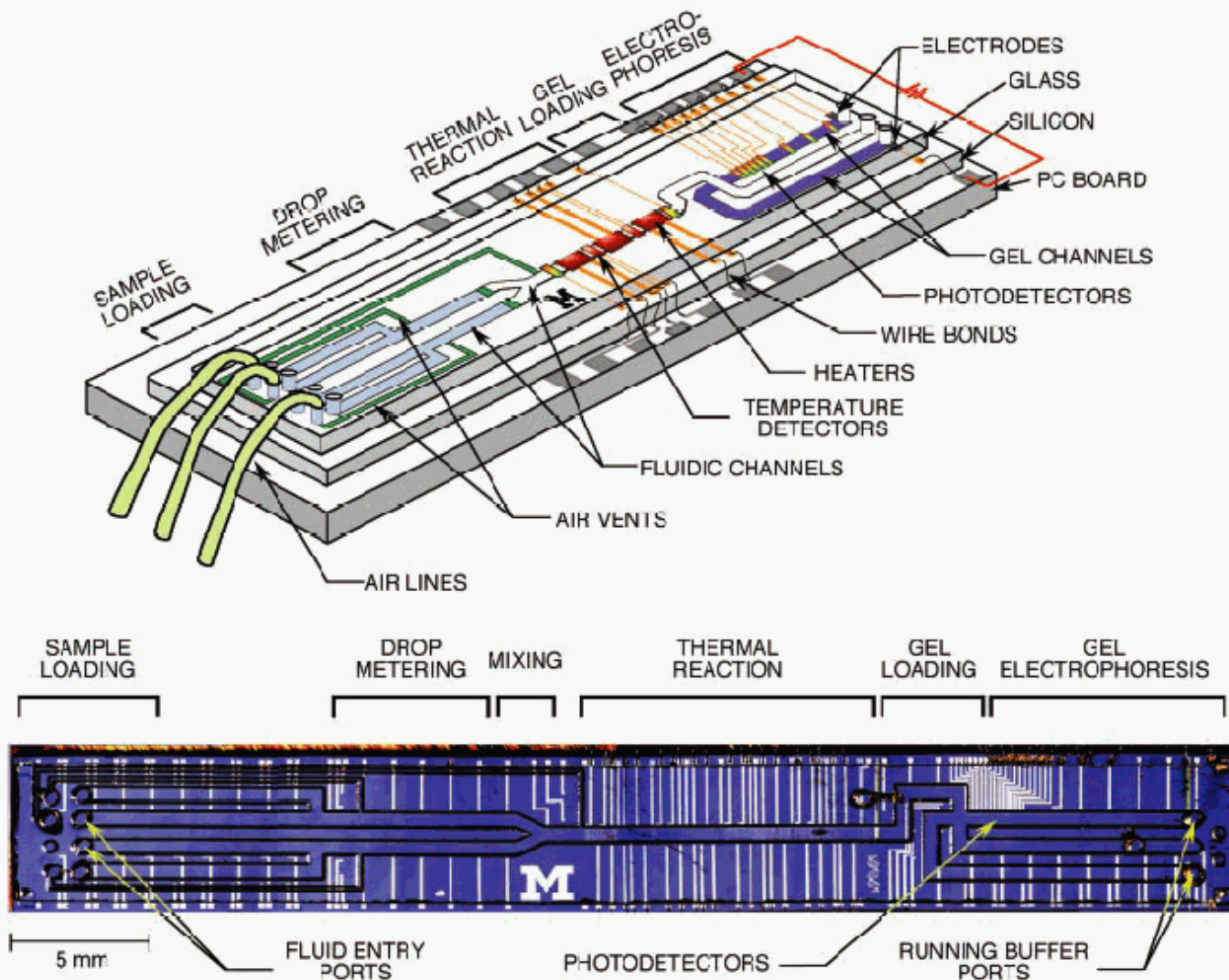
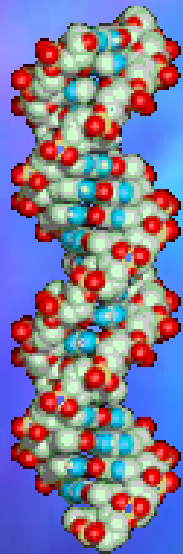



# MIT Micro-turbomachinery



*Fig. 16: Micro-turbine rotor-stator combination.  
This comprises the middle wafer of the 5-wafer stack shown above.  
The rotor is 4mm in diameter.*

# Lab on Chip





# End